NSS40300DDR2G

Dual 40 V, 6.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e^2PowerEdge family of low $V_{CE(sat)}$ transistors are surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e^2PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- Halide Free
- This is a Pb−Free Device

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	−40	Vdc
Collector-Base Voltage	V_{CBO}	−40	Vdc
Emitter-Base Voltage	V_{EBO}	−7.0	Vdc
Collector Current − Continuous	I_C	−3.0	A
Collector Current − Peak	I_{CM}	−6.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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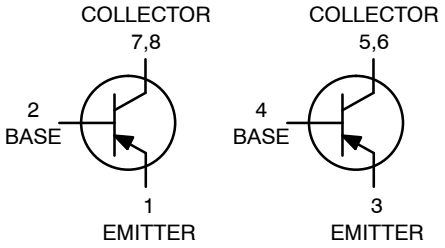
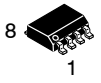
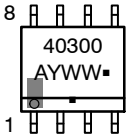
40 VOLTS
6.0 AMPS
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 80 mΩ





SOIC−8
CASE 751
STYLE 16

DEVICE MARKING



40300 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSS40300DDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
SINGLE HEATED			
Total Device Dissipation (Note 1) T_A = 25°C Derate above 25°C	P_D	576 4.6	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	217	°C/W
Total Device Dissipation (Note 2) T_A = 25°C Derate above 25°C	P_D	676 5.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	185	°C/W
DUAL HEATED (Note 3)			
Total Device Dissipation (Note 1) T_A = 25°C Derate above 25°C	P_D	653 5.2	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	191	°C/W
Total Device Dissipation (Note 2) T_A = 25°C Derate above 25°C	P_D	783 6.3	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	160	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ 10 mm^2, 1 oz. copper traces, still air.
2. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
3. Dual heated values assume total power is the sum of two equally powered devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−40	–	–	Vdc
Collector – Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−40	–	–	Vdc
Emitter – Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−7.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = −40 Vdc, I_E = 0)	I_{CBO}	–	–	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −6.0 Vdc)	I_{EBO}	–	–	−0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = −10 mA, V_{CE} = −2.0 V) (I_C = −500 mA, V_{CE} = −2.0 V) (I_C = −1.0 A, V_{CE} = −2.0 V) (I_C = −2.0 A, V_{CE} = −2.0 V)	h_{FE}	 250 220 180 150	 380 340 300 230	 – – – –	
Collector – Emitter Saturation Voltage (Note 4) (I_C = −0.1 A, I_B = −0.010 A) (I_C = −1.0 A, I_B = −0.100 A) (I_C = −1.0 A, I_B = −0.010 A) (I_C = −2.0 A, I_B = −0.200 A)	$V_{CE(sat)}$	 – – – –	 −0.013 −0.075 −0.130 −0.135	 −0.017 −0.095 −0.170 −0.170	V
Base – Emitter Saturation Voltage (Note 4) (I_C = −1.0 A, I_B = −0.01 A)	$V_{BE(sat)}$	–	−0.780	−0.900	V
Base – Emitter Turn−on Voltage (Note 4) (I_C = −0.1 A, V_{CE} = −2.0 V)	$V_{BE(on)}$	–	−0.660	−0.750	V
Cutoff Frequency (I_C = −100 mA, V_{CE} = −5.0 V, f = 100 MHz)	f_T	100	–	–	MHz
Input Capacitance (V_{EB} = −0.5 V, f = 1.0 MHz)	Cibo	–	250	300	pF
Output Capacitance (V_{CB} = −3.0 V, f = 1.0 MHz)	Cobo	–	50	65	pF
SWITCHING CHARACTERISTICS					
Delay (V_{CC} = −30 V, I_C = −750 mA, I_{B1} = −15 mA)	t_d	–	–	60	ns
Rise (V_{CC} = −30 V, I_C = −750 mA, I_{B1} = −15 mA)	t_r	–	–	120	ns
Storage (V_{CC} = −30 V, I_C = −750 mA, I_{B1} = −15 mA)	t_s	–	–	400	ns
Fall (V_{CC} = −30 V, I_C = −750 mA, I_{B1} = −15 mA)	t_f	–	–	130	ns

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

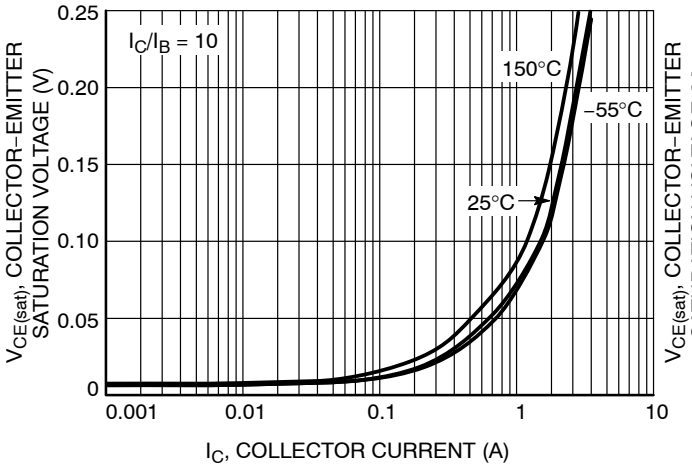


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

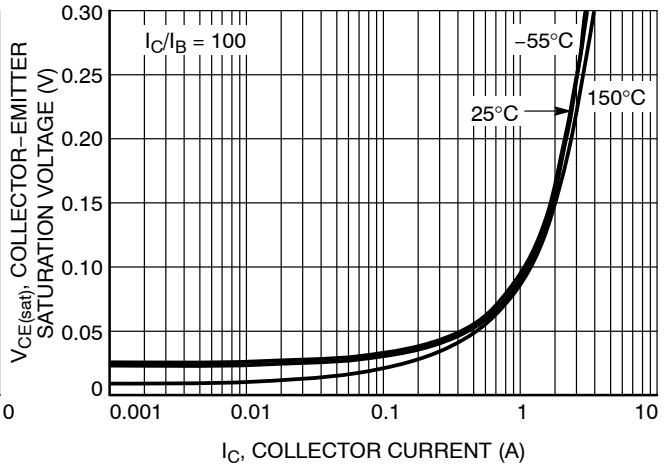


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

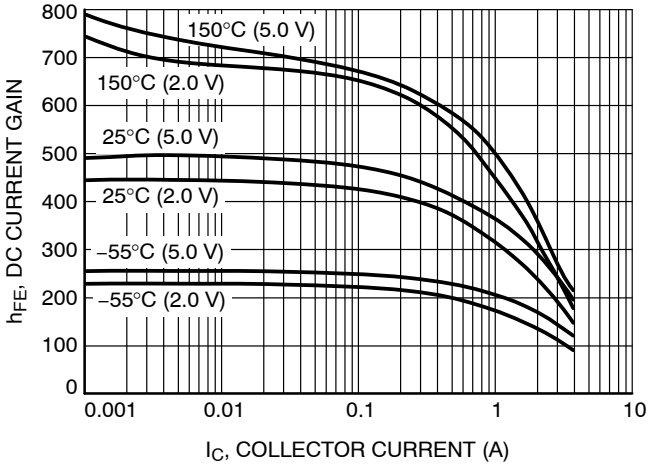


Figure 3. DC Current Gain vs. Collector Current

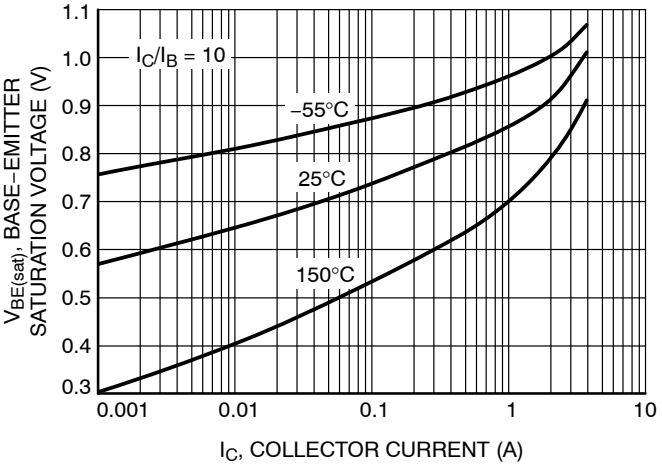


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

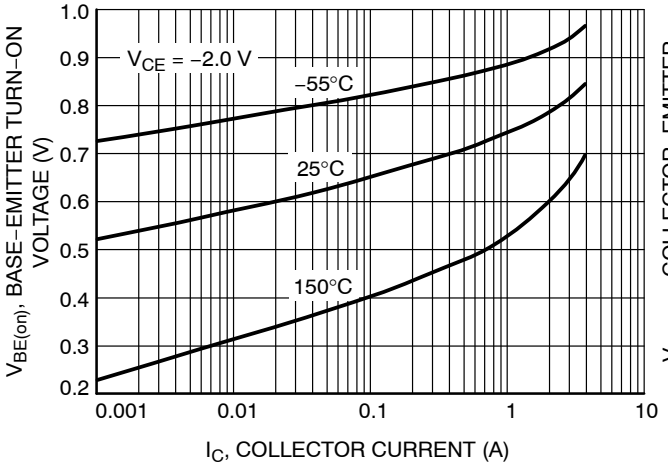


Figure 5. Base Emitter Turn−On Voltage vs. Collector Current

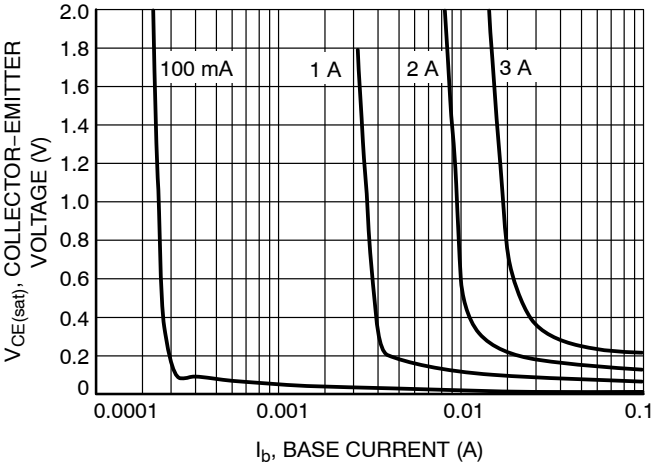


Figure 6. Saturation Region

TYPICAL CHARACTERISTICS

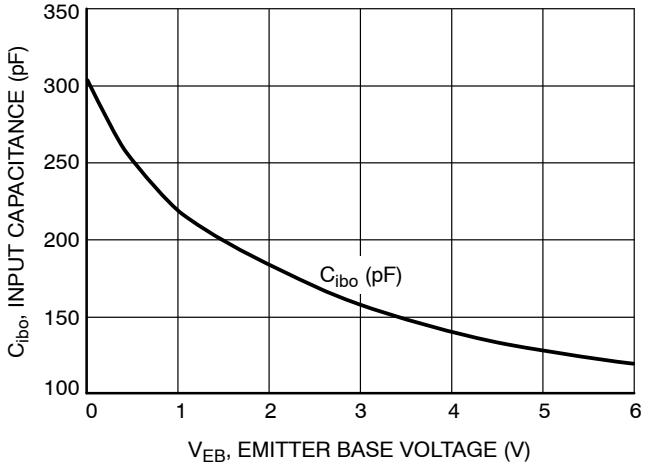


Figure 7. Input Capacitance

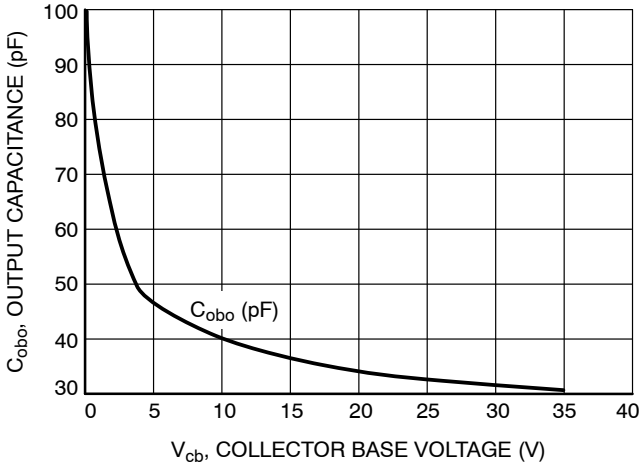


Figure 8. Output Capacitance

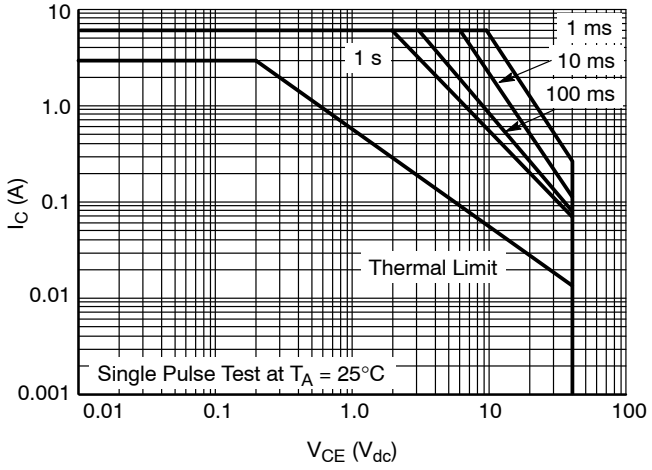
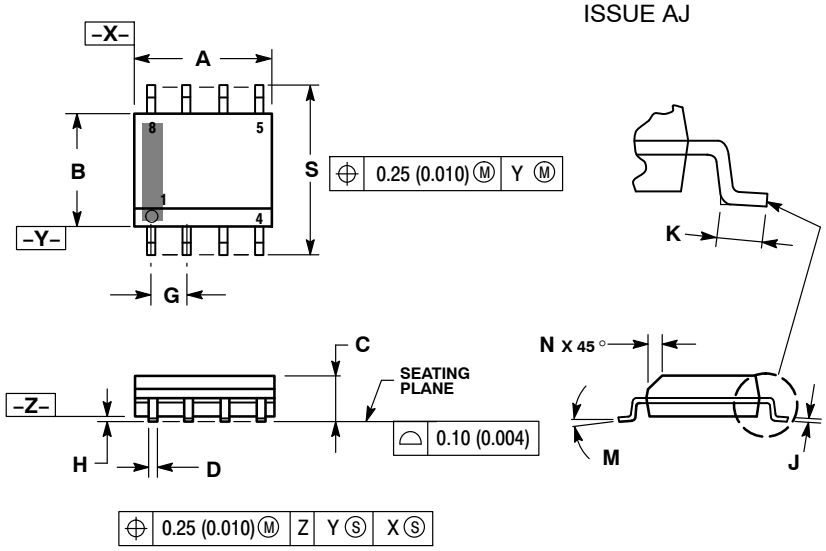


Figure 9. Safe Operating Area

NSS40300DDR2G

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AJ

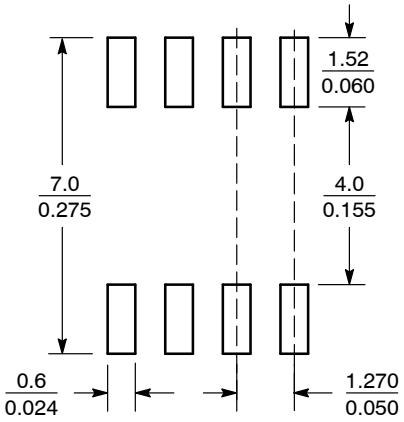


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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