PCA9571

Remote 8-bit general purpose outputs for 1 MHz I²C-bus

Rev. 1 — 22 December 2014 Product data sheet

1. General description

The PCA9571 is a CMOS device that provide 8 bits of General Purpose parallel Output (GPO) expansion in low voltage processor and handheld battery powered mobile applications. They operate at 1 MHz I²C-bus speeds on a lightly loaded bus (<100 pF) while maintaining backward compatibility to Fast-mode (400 kHz) and Standard-mode (100 kHz).

The PCA9571 is a streamlined GPO that consists of 8-bit push-pull outputs that offer low current consumption, small packaging options and a low operating voltage range of 1.1 V to 3.6 V. The latched outputs are symmetrical 4 mA current drive capability at 3.3 V to drive various control logic. The PCA9571 output expanders provide a simple solution when additional outputs are needed while keeping interconnections and floor space to a minimum, for example, in battery powered mobile applications where PCBs are crowded for interfacing to sensors, push buttons, etc.

The PCA9571 contains an internal Power-On Reset (POR) and a Software Reset feature that initializes the device to its default state.

2. Features and benefits

- 1 MHz I²C-bus interface with 6 mA SDA sink capability for lightly loaded buses (<100 pF) and improved power consumption
- Compliant with the I²C-bus Fast and Standard modes
- 1.1 V to 3.6 V operation
- Latched outputs with a sink/source capability of 4 mA at 3.3 V
- Readable device ID (manufacturer, device type, and revision)
- Software Reset
- Power-On Reset
- Low standby current
- –40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: XQFN12, TSSOP14 and DHVQFN14

3. Applications

- Smartphones and tablets
- Portable medical equipment
- Portable instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9571GU	71	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 × 2.00 × 0.50 mm	SOT1174-1
PCA9571BQ[1]	P9571	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
PCA9571PW[1]	PCA9571	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

[1] In development. Contact your NXP sales office for availability.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9571GU	PCA9571GUX	XQFN12	Reel 7” Q1/T1 *standard mark SMD	4000	T_{amb} = −40 °C to +85 °C
PCA9571BQ[1]	PCA9571BQX	DHVQFN14	Reel 7” Q1/T1 *standard mark SMD	3000	T_{amb} = −40 °C to +85 °C
PCA9571PW[1]	PCA9571PWJ	TSSOP14	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

[1] In development. Contact your NXP sales office for availability.

5. Block diagram

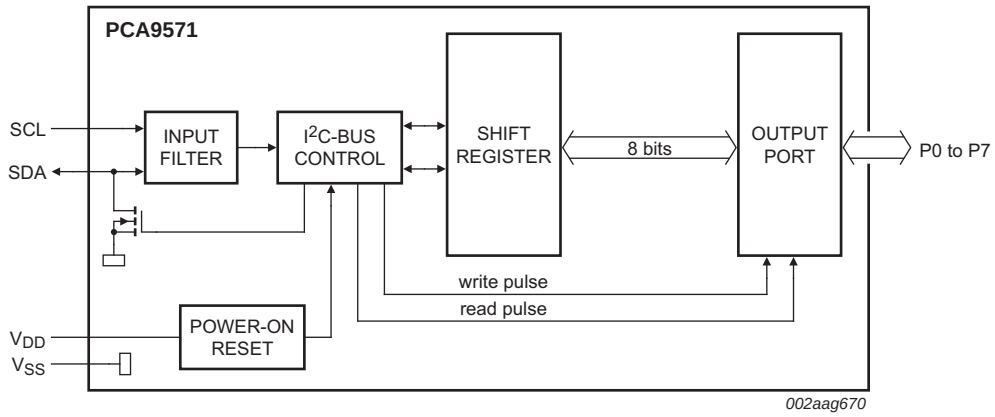


Fig 1. Block diagram of PCA9571

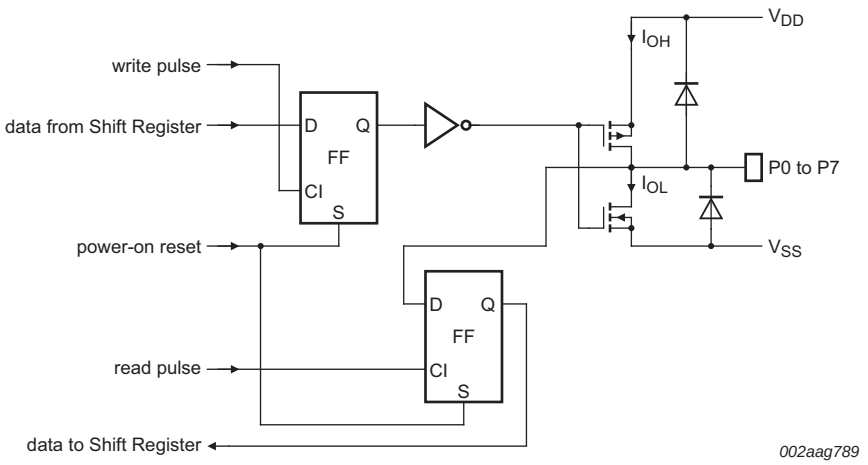


Fig 2. Simplified schematic of the I/Os (P0 to P7)

6. Pinning information

6.1 Pinning

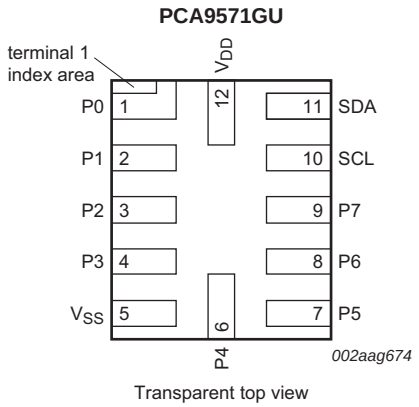


Fig 3. Pin configuration for XQFN12

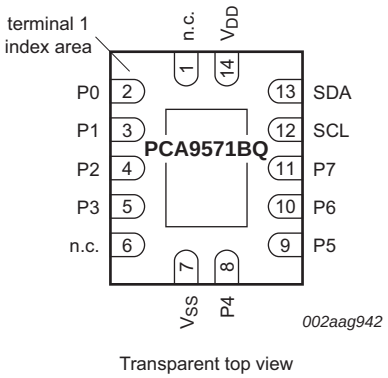


Fig 4. Pin configuration for DHVQFN14

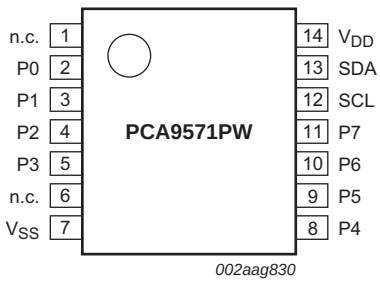


Fig 5. Pin configuration for TSSOP14

6.2 Pin description

Table 3. Pin description for XQFN12

Symbol	Pin	Description
P0	1	output 0
P1	2	output 1
P2	3	output 2
P3	4	output 3
V_{SS}	5	supply ground
P4	6	output 4
P5	7	output 5
P6	8	output 6
P7	9	output 7
SCL	10	serial clock line
SDA	11	serial data line
V_{DD}	12	supply voltage

Table 4. Pin description for TSSOP14, DHVQFN14

Symbol	Pin	Description
n.c.	1	not connected
P0	2	output 0
P1	3	output 1
P2	4	output 2
P3	5	output 3
n.c.	6	not connected
V_{SS}	7	supply ground
P4	8	output 4
P5	9	output 5
P6	10	output 6
P7	11	output 7
SCL	12	serial clock line
SDA	13	serial data line
V_{DD}	14	supply voltage

7. Functional description

Refer to Figure 1 “Block diagram of PCA9571”.

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9571 is 4Ah as shown in Figure 6.

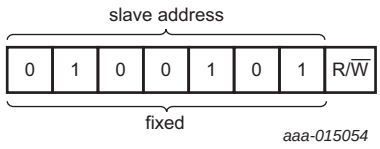


Fig 6. PCA9571 device address

7.2 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows to reset the device through the I²C-bus upon reception of the right I²C-bus sequence. See Section 7.2.1 “Software Reset” for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 7.2.2 “Device ID (PCA9571 ID field)” for more information.

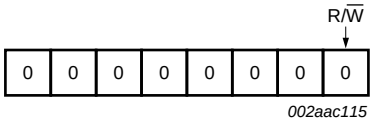


Fig 7. General Call address

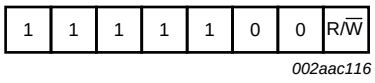


Fig 8. Device ID address

7.2.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address ‘0000 000’ with the R/$\overline{W}$ bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address ‘0000 0000’ (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.

4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

   If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 9.

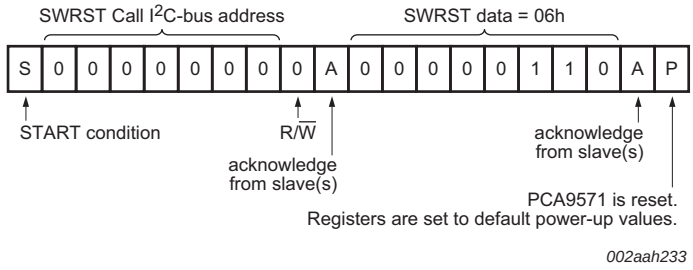


Fig 9. Software Reset sequence

7.2.2 Device ID (PCA9571 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer, the 7 MSBs with the category ID and the 6 LSBs with the feature ID (for example PCA9571 8-bit I/O expander).
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 0 (write): ‘1111 1000’.
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a ‘Don’t care’ value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.
5. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 1 (read): ‘1111 1001’.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

   Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

   If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

   PCA9571 Device ID is shown in Figure 10.

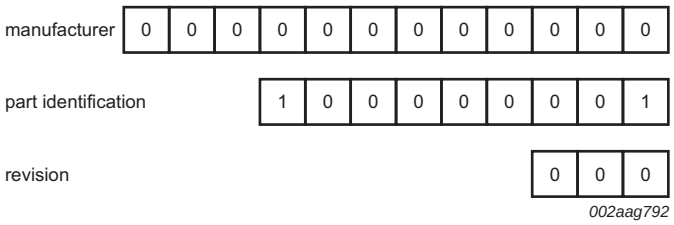
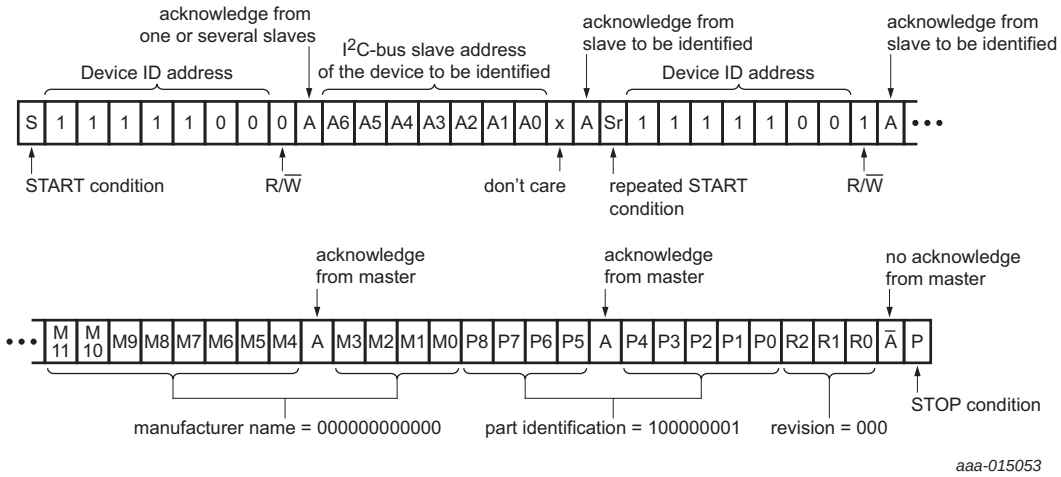


Fig 10. PCA9571 Device ID field



If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 11. Device ID field reading

8. I/O programming

8.1 I/O architecture

The device's ports (see Figure 2) are entirely independent and are output ports. The state of the ports at the pin is transferred from the ports to the microcontroller in the Read mode (see Figure 13). Output data is transmitted to the ports in the Write mode (see Figure 12).

At power-on all ports are HIGH. The state of the Output Port register determines if either Q1 or Q2 is on, driving the line either HIGH or LOW. A bit set to 1 in the data byte will drive the line HIGH at the corresponding port. A bit set to 0 in the data byte will drive the line LOW at the corresponding port.

If an external voltage is applied to an output, care should be exercised because of the low-impedance path that exists between the pin and either V_{DD} or V_{SS}.

8.2 Writing to the port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the Write mode is entered. The device acknowledges and the master sends the data byte for P7 to P0 and is acknowledged by the device. The 8-bit data is presented on the port lines after it has been acknowledged by the device. The number of data bytes that can be sent successively is not limited. The previous data is overwritten every time a data byte has been sent.

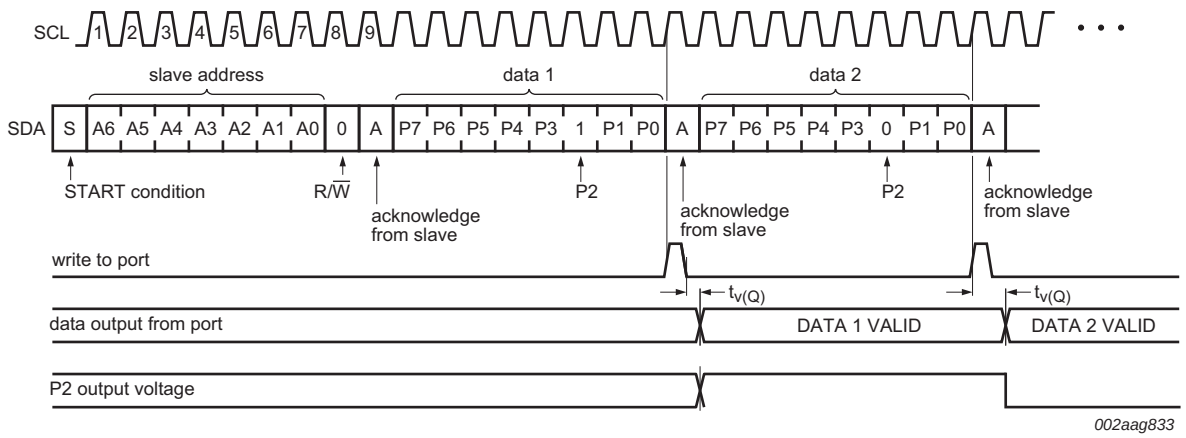


Fig 12. Write mode (output)

8.3 Reading from a port (Input mode)

All ports are outputs and cannot be used as inputs. When reading the device, the data returned is the port state at the pin. To read, the master (microcontroller) first addresses the slave device by setting the last bit of the byte containing the slave address to logic 1. The data byte that follows on the SDA is the value of the ports pins. There is no limit to the number of bytes read, and the state of the output port pins is updated at each acknowledge cycle. Logic 1 means that the port is HIGH. Logic 0 means that the port is LOW.

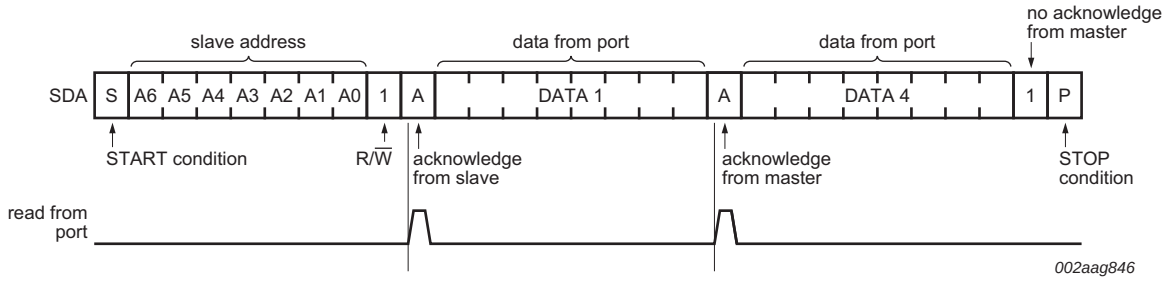


Fig 13. Read input port register

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the device in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the device registers and I²C-bus/SMBus state machine will initialize to their default states. See Section 13 for DC and AC characteristics of the POR function.

9. Application design-in information

9.1 I/O expander applications

Figure 14 shows an 8-bit output expander application. The desired HIGH or LOW logic levels are controlled by the master with speeds of up to 1 MHz on a lightly loaded bus (<100 pF). This allows the host processor to control various functions quickly and with very low overhead. The port read function of the device enables the host processor to poll the status of the output port pins. This is useful for system recovery operations or debugging.

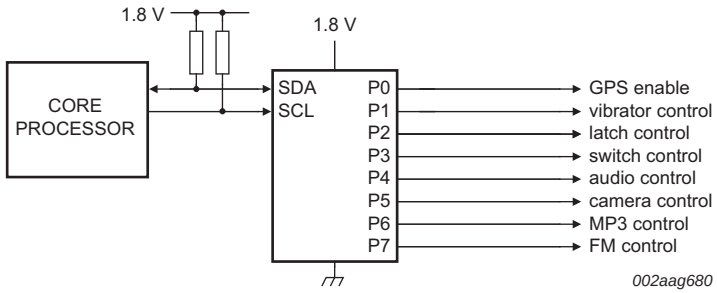


Fig 14. I/O expander application

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+4	V
V_I	input voltage	SCL; SDA [1]	−0.5	+4	V
I_{IK}	input clamping current	SCL; $V_I < 0$ V	-	±18	mA
I_{OK}	output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD}$	-	±18	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD}$	-	±18	mA
I_O	output current	continuous; P port	-	±25	mA
I_{OL}	LOW-level output current	continuous; SDA; V_O = 0 V to V_{DD}	-	25	mA
I_{DD}	supply current	continuous through V_{SS}	-	100	mA
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

11. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.1 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA	−1.2	-	-	V
V_{DD}	supply voltage		1.1	-	3.6	V
V_{POR}	power-on reset voltage	$V_I = V_{DD}$ or V_{SS}; I_O = 0 mA	-	0.7	1.0	V
V_{OL}	LOW-level output voltage	P port; I_{OL} = 2 mA; V_{DD} = 1.65 V	-	-	0.25	V
		P port; I_{OL} = 3 mA; V_{DD} = 2.3 V	-	-	0.25	V
		P port; I_{OL} = 4 mA; V_{DD} = 3 V	-	-	0.25	V
V_{OH}	HIGH-level output voltage	P port; I_{OL} = 2 mA; V_{DD} = 1.65 V	1.35	-	-	V
		P port; I_{OL} = 3 mA; V_{DD} = 2.3 V	2.0	-	-	V
		P port; I_{OL} = 4 mA; V_{DD} = 3 V	2.7	-	-	V
I_{OL}	LOW-level output current	SDA; V_{OL} = 0.4 V; V_{DD} = 2.1 V to 3.6 V	3	-	-	mA
		SDA; $V_{OL} = 0.2 \times V_{DD}$; V_{DD} = 1.1 V to 2.0 V	1	-	-	mA
V_{IH}	HIGH-level input voltage	SCL, SDA; V_{DD} = 1.1 V to 1.2 V	$0.8 \times V_{DD}$	-	1.2	V
		SCL, SDA; V_{DD} = 1.2 V to 3.6 V	$0.7 \times V_{DD}$	-	3.6	V
V_{IL}	LOW-level input voltage	SCL, SDA; V_{DD} = 1.1 V to 1.2 V	−0.5	-	$0.2 \times V_{DD}$	V
		SCL, SDA; V_{DD} = 1.2 V to 3.6 V	−0.5	-	$0.3 \times V_{DD}$	V
I_I	input current	SCL, SDA; V_{DD} = 1.1 V to 3.6 V; $V_I = V_{DD}$ or V_{SS}	-	-	±1	µA
I_{DD}	supply current	SDA, P port; V_I on SDA = V_{DD} or V_{SS}; I_O = 0 mA; f_{SCL} = 400 kHz				
		V_{DD} = 2.3 V to 3.6 V	-	6.5	15	µA
		V_{DD} = 1.1 V to 2.3 V	-	4	9	µA
		SCL, SDA, P port; V_I on SCL, SDA = V_{DD} or V_{SS}; I_O = 0 mA; f_{SCL} = 0 kHz				
		V_{DD} = 2.3 V to 3.6 V	-	1	3.2	µA
		V_{DD} = 1.1 V to 2.3 V	-	0.6	1.7	µA
		Active mode: SCL, SDA, P port; I_O = 0 mA; f_{SCL} = 400 kHz; continuous register read				
		V_{DD} = 1.1 V to 3.6 V	-	50	75	µA
C_i	input capacitance	$V_I = V_{DD}$ or V_{SS}	-	6	7	pF
C_o	output capacitance	$V_O = V_{DD}$ or V_{SS}	-	3	5	pF
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

[1] The typical values are at V_{DD} = 2.2 V and T_{amb} = 25 °C.

11.1 Typical characteristics

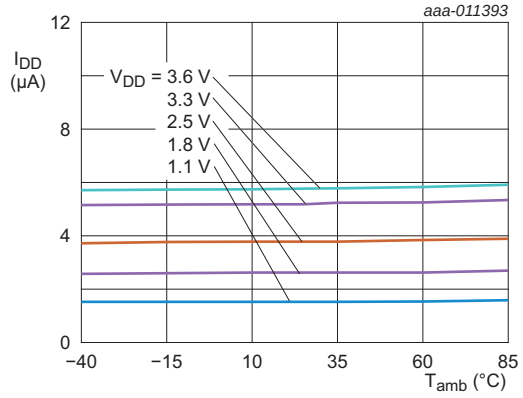


Fig 15. Supply current versus ambient temperature

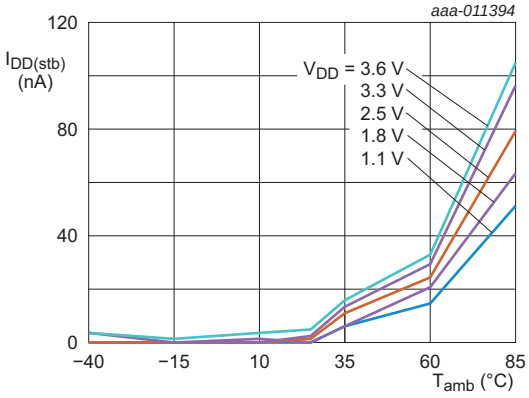
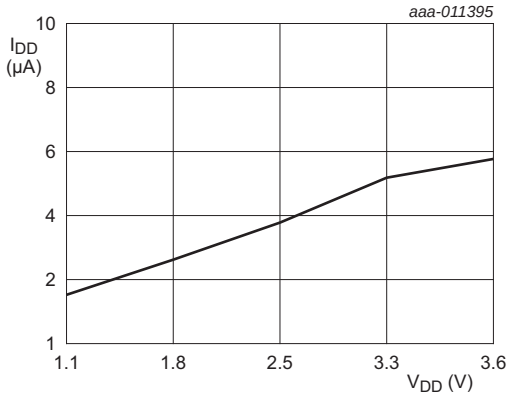
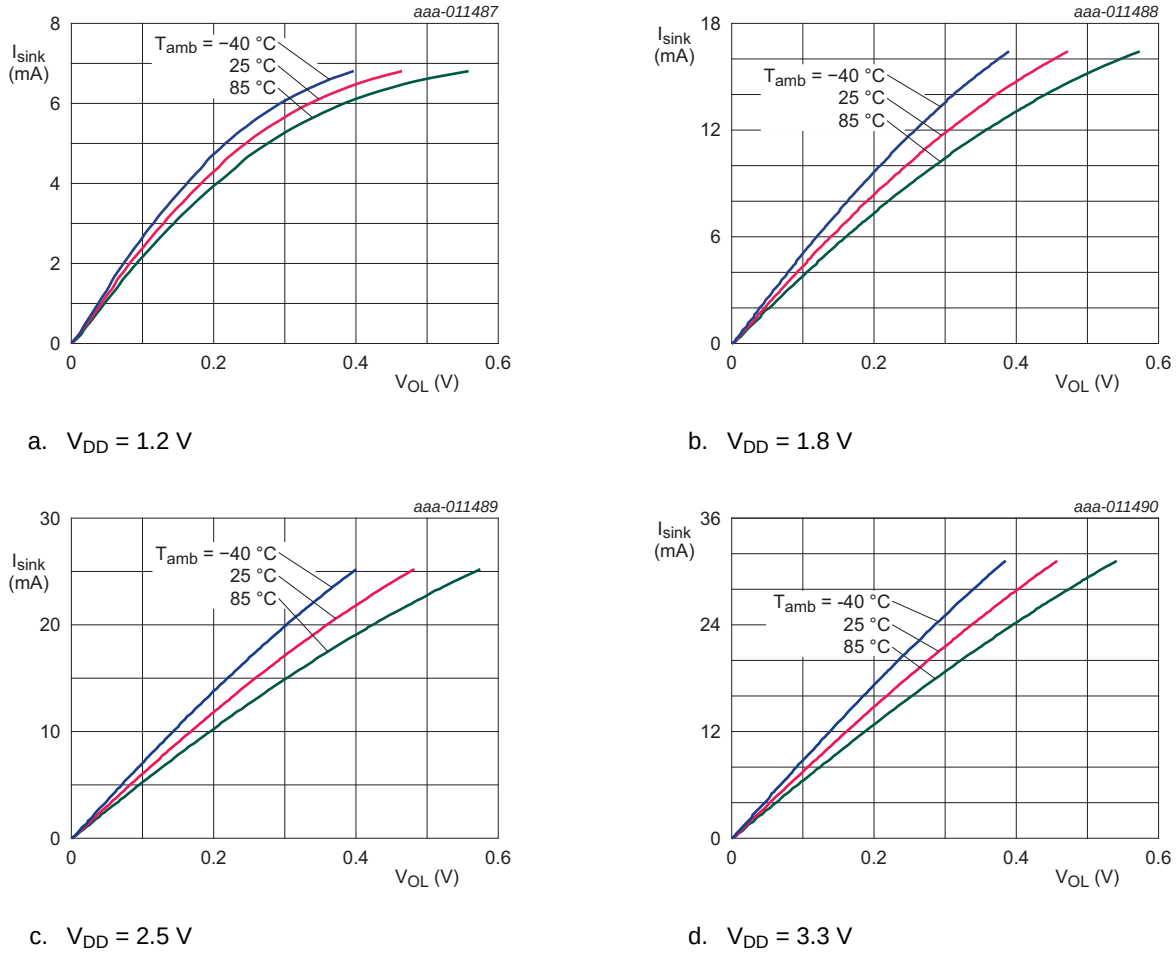


Fig 16. Standby supply current versus ambient temperature



T_{amb} = 25 °C

Fig 17. Supply current versus supply voltage



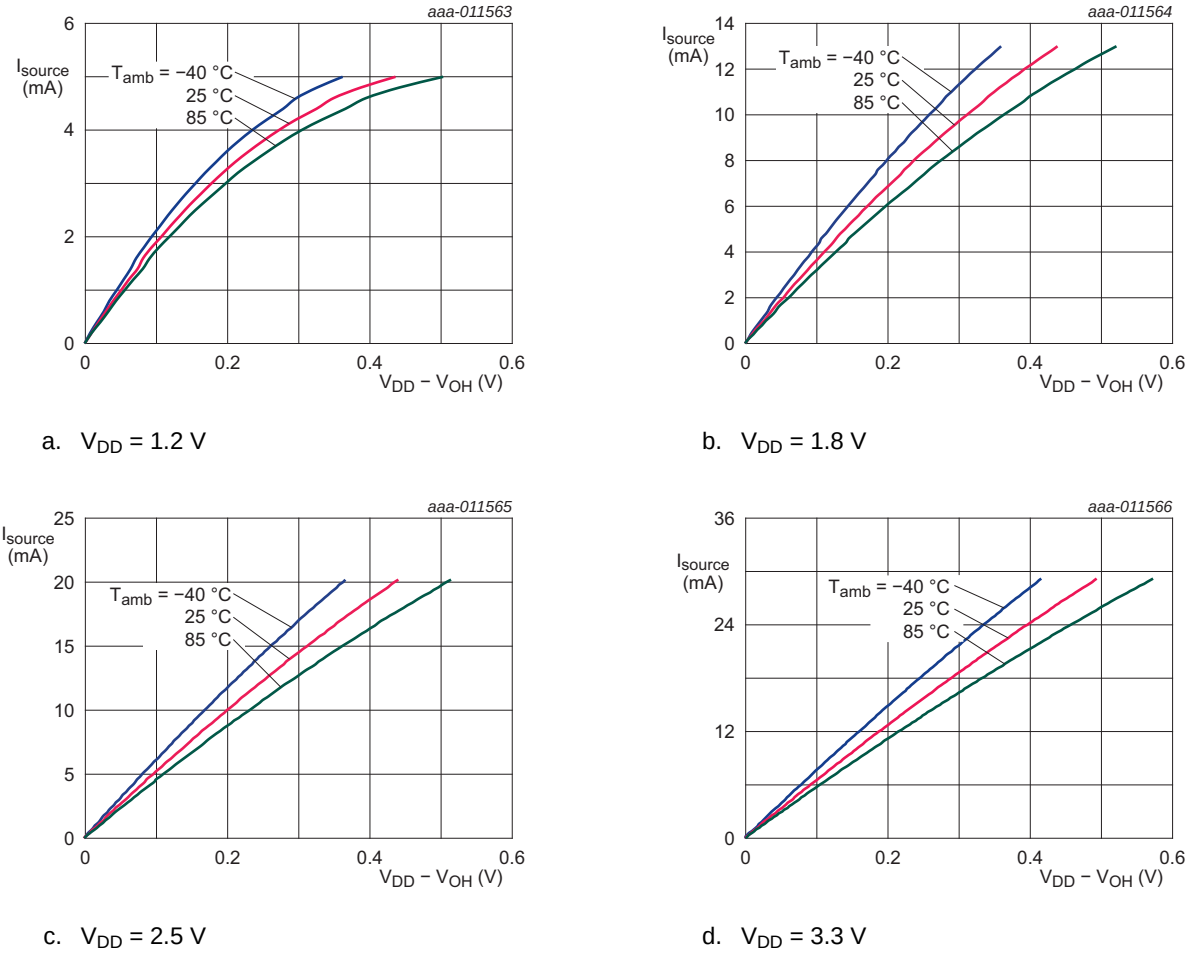
a. V_{DD} = 1.2 V

b. V_{DD} = 1.8 V

c. V_{DD} = 2.5 V

d. V_{DD} = 3.3 V

Fig 18. I/O sink current versus LOW-level output voltage



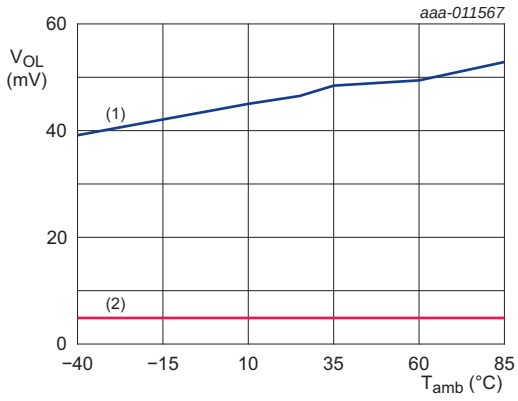
a. V_{DD} = 1.2 V

b. V_{DD} = 1.8 V

c. V_{DD} = 2.5 V

d. V_{DD} = 3.3 V

Fig 19. I/O source current versus HIGH-level output voltage



(1) V_{DD} = 1.8 V; I_{sink} = 2 mA

(2) V_{DD} = 1.8 V; I_{sink} = 100 μA

Fig 20. LOW-level output voltage versus temperature

12. Dynamic characteristics

Table 7. Dynamic characteristics

V_{DD} = 1.1 V to 3.6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I²C-bus		Fast mode I²C-bus		1 MHz I²C-bus[1]		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[2]	-	3.45	-	0.9	-	0.45	µs
$t_{VD;DAT}$	data valid time	[3]	-	3.45	-	0.9	-	0.45	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals		-	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[4]	-	50	-	50	-	50	ns
Port timing									
$t_{v(Q)}$	data output valid time		-	200	-	200	-	200	ns

[1] Fm+ mode on a non-standard, lightly loaded bus (<100 pF).

[2] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[3] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[4] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

13. Power-on reset requirements

In the event of a glitch or data corruption, the device can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

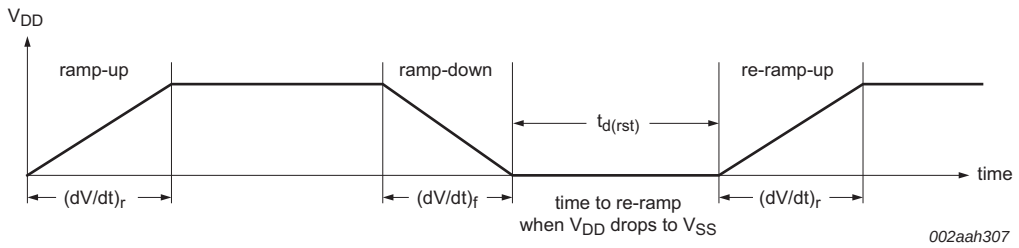


Fig 21. V_{DD} is lowered below 0.6 V and then ramped up to V_{DD}

Table 8. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 21	0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 21	0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 21; when V_{DD} drops to V_{SS}	1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 22 [1]				
		V_{DD} = 2.1 V to 3.6 V	-	-	1.2	V
		V_{DD} = 1.1 V to 2.1 V	-	-	V_{DD} − 0.9	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 22 [2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	rising V_{DD}	-	0.7	1.0	V

[1] Level that V_{DD} can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ = 1 µs.

[2] Glitch width that will not cause a functional disruption when V_{DD} = 1.8 V to 3.6 V, $\Delta V_{DD(gl)} = 0.5 \times V_{DD}$; V_{DD} = 1.1 V to 1.8 V, $\Delta V_{DD(gl)} = V_{DD} - 0.9$ V.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 22 and Table 8 provide more information on how to measure these specifications.

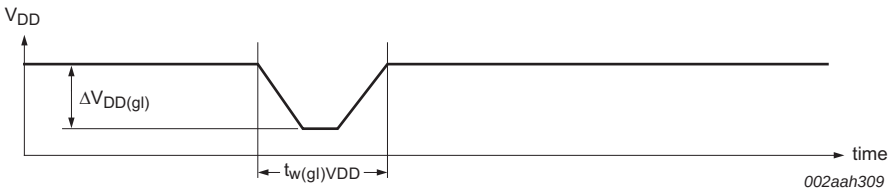


Fig 22. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C-bus/SMBus state machine are initialized to their default states. Figure 23 and Table 8 provide more details on this specification.

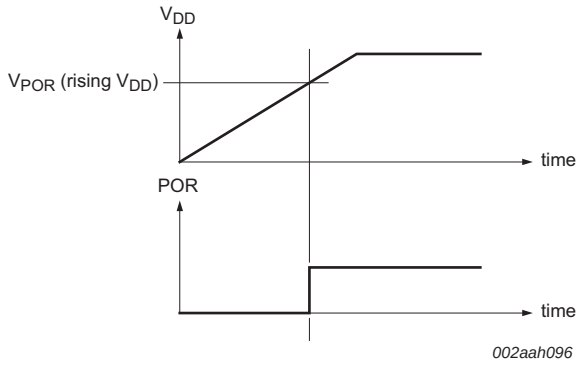
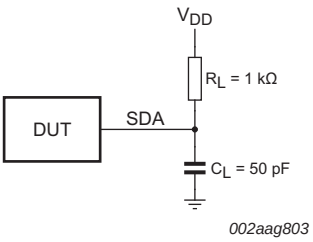
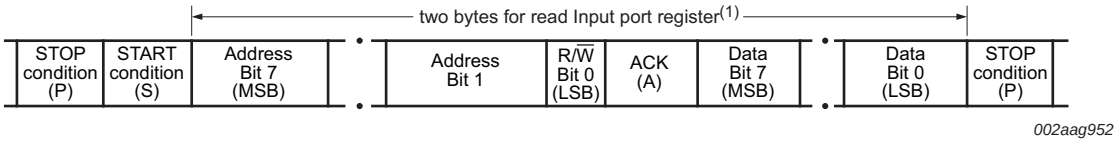


Fig 23. Power-on reset voltage (V_{POR})

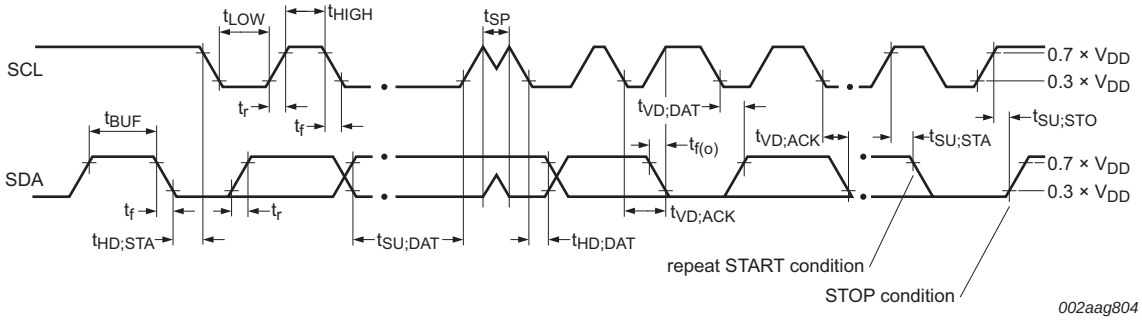
14. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance.

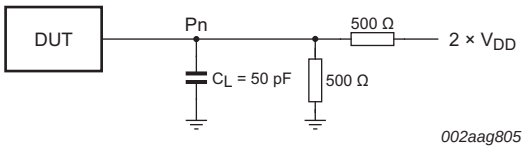
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

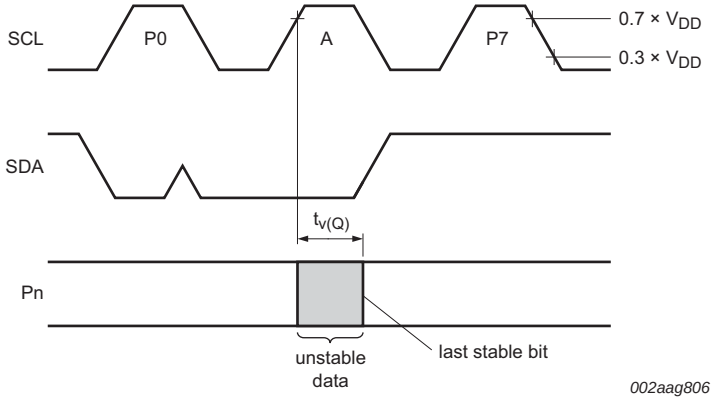
Byte 1 = I²C-bus address; Byte 2, byte 3 = P port data.

(1) See Figure 13.

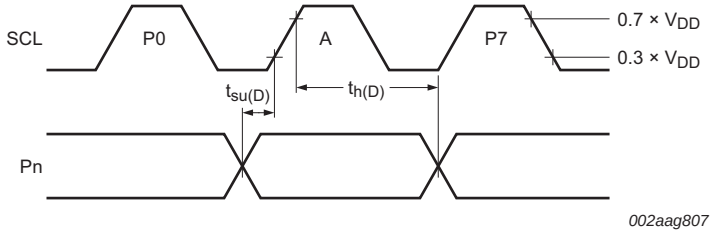
Fig 24. I²C-bus interface load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

$t_{v(Q)}$ is measured from 0.7 × V_{DD} on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

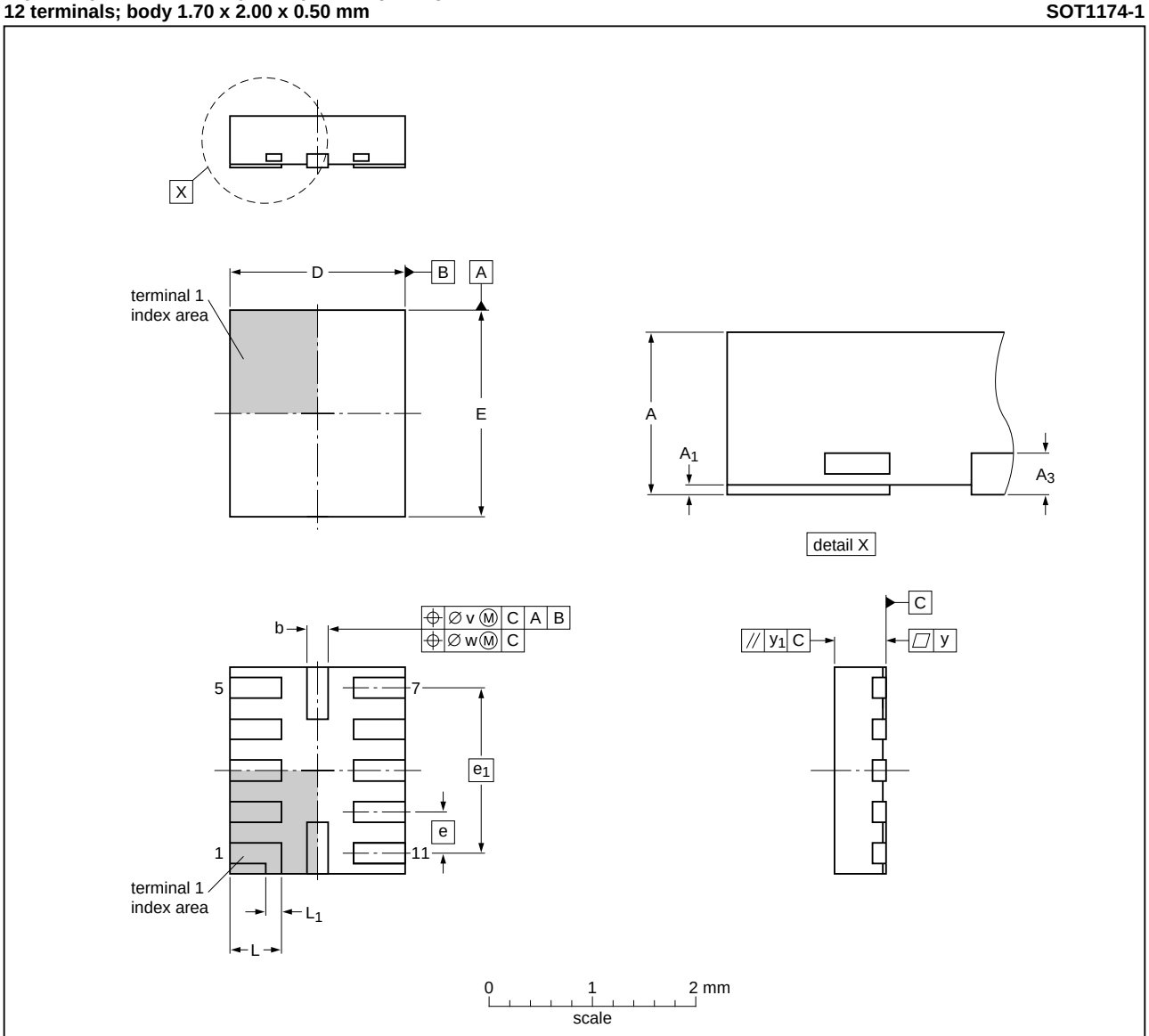
The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 25. P port load circuit and voltage waveforms

15. Package outline

XQFN12: plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 x 2.00 x 0.50 mm **SOT1174-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.8	2.1			0.55					
mm	nom			0.127	0.20	1.7	2.0	0.4	1.6	0.50	0.15	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.6	1.9			0.45					

Note

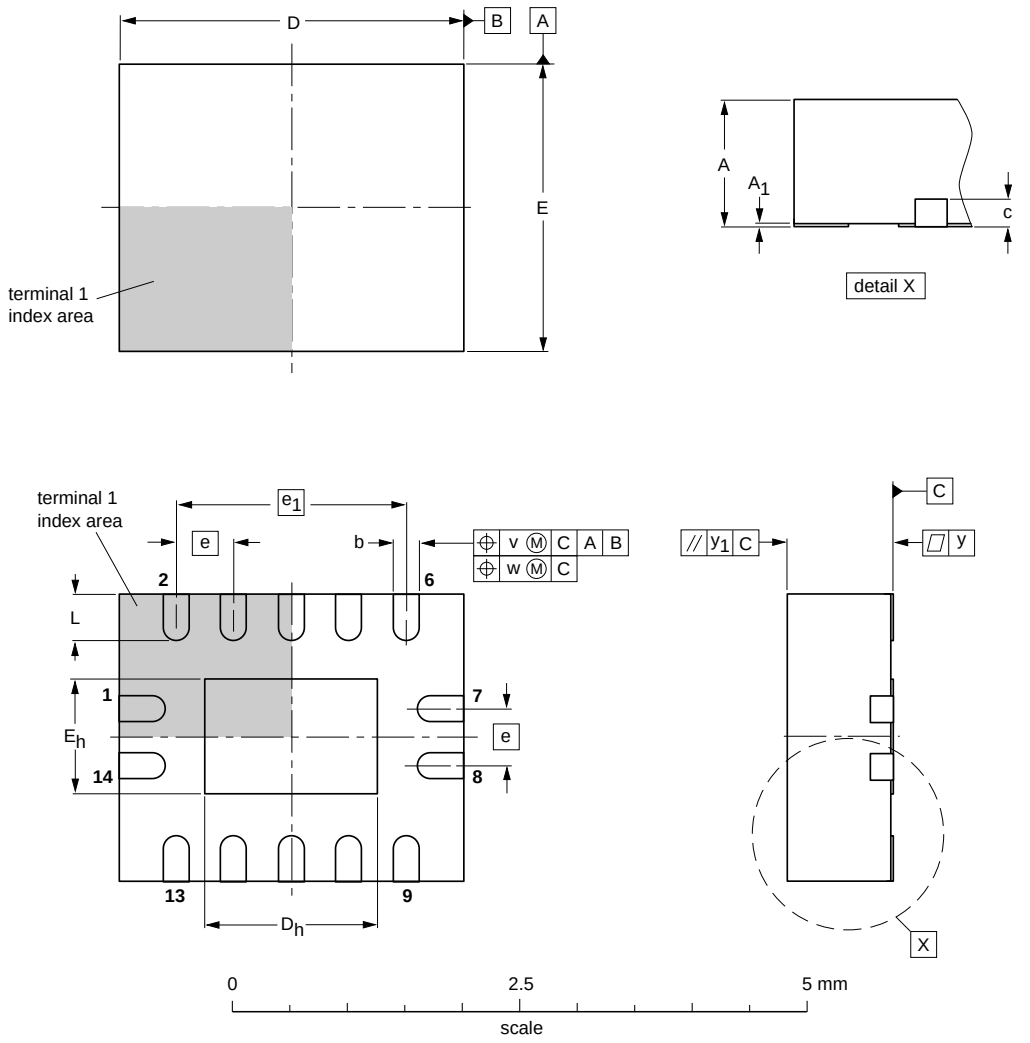
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1174-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1174-1	- - -	MO-288	- - -			10-04-07 10-04-21

Fig 26. Package outline SOT1174-1 (XQFN12)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

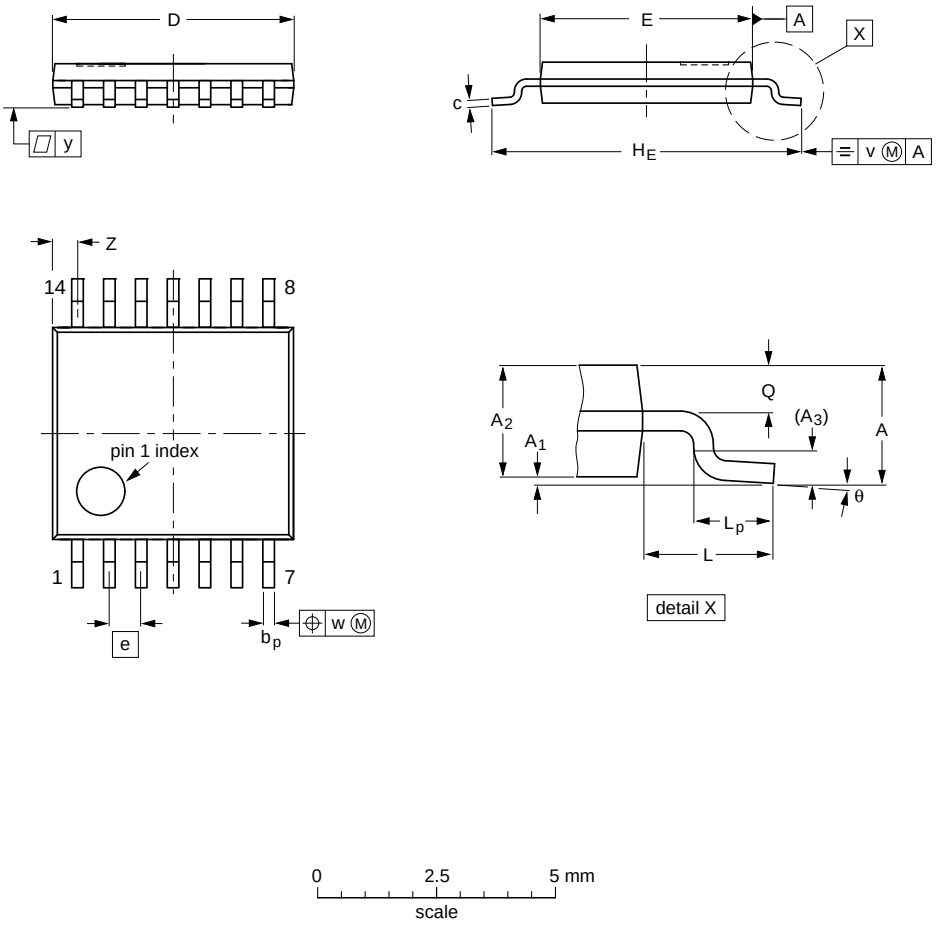
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 27. Package outline SOT762-1 (DHVQFN14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 28. Package outline SOT402-1 (TSSOP14)

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020D)

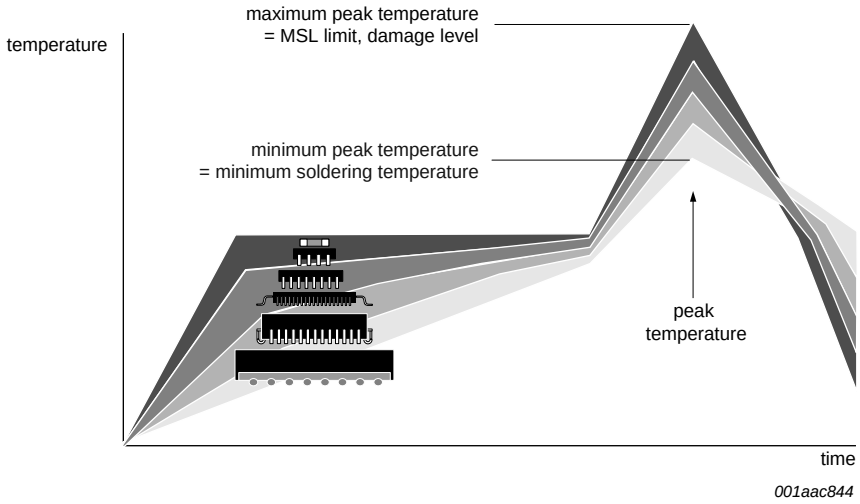
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.



MSL: Moisture Sensitivity Level

Fig 29. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Soldering: PCB footprints

Footprint information for reflow soldering of XQFN12 package **SOT1174-1**

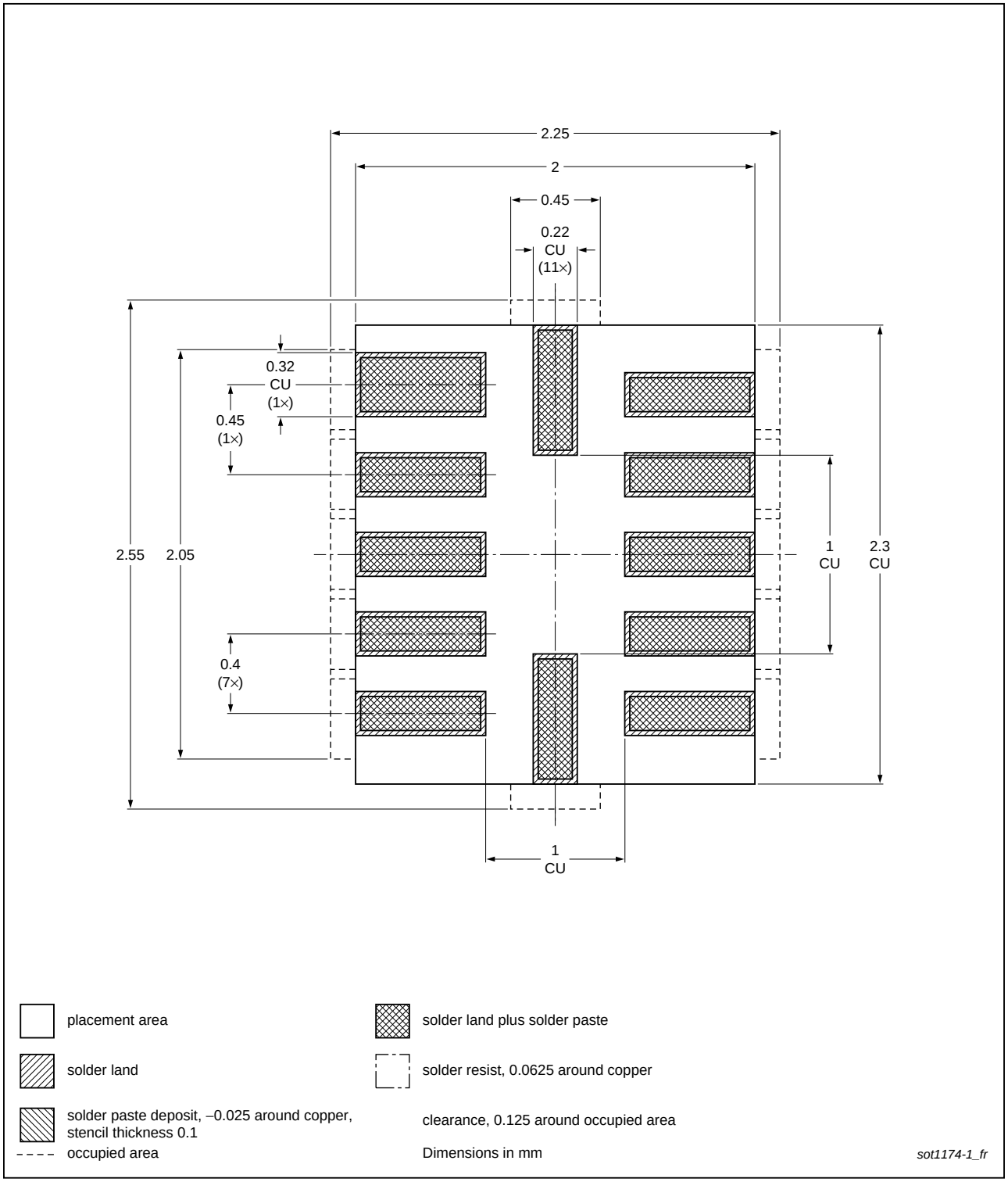


Fig 30. PCB footprint for SOT1174-1 (XQFN12); reflow soldering

Footprint information for reflow soldering of DHVQFN14 package **SOT762-1**

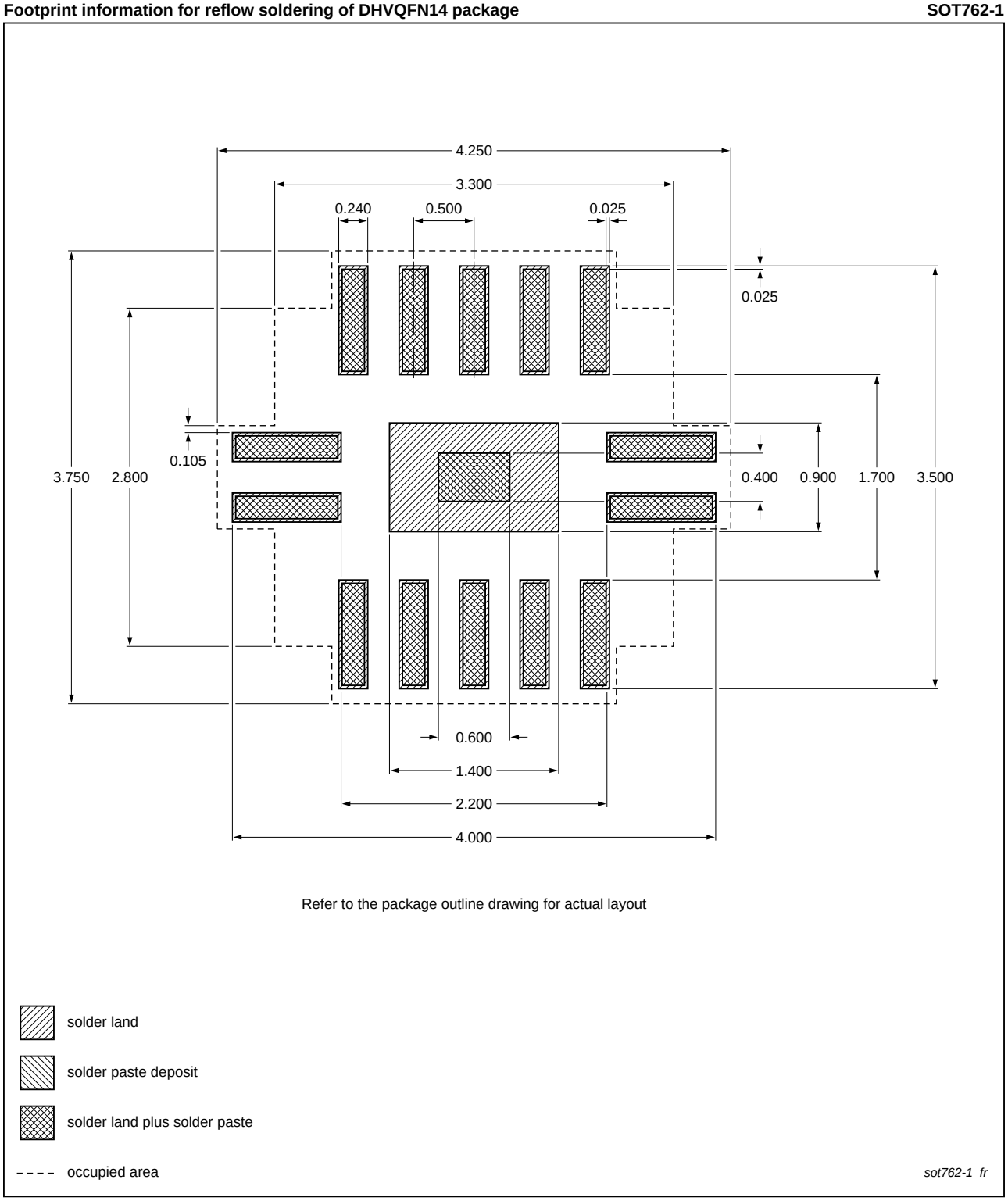
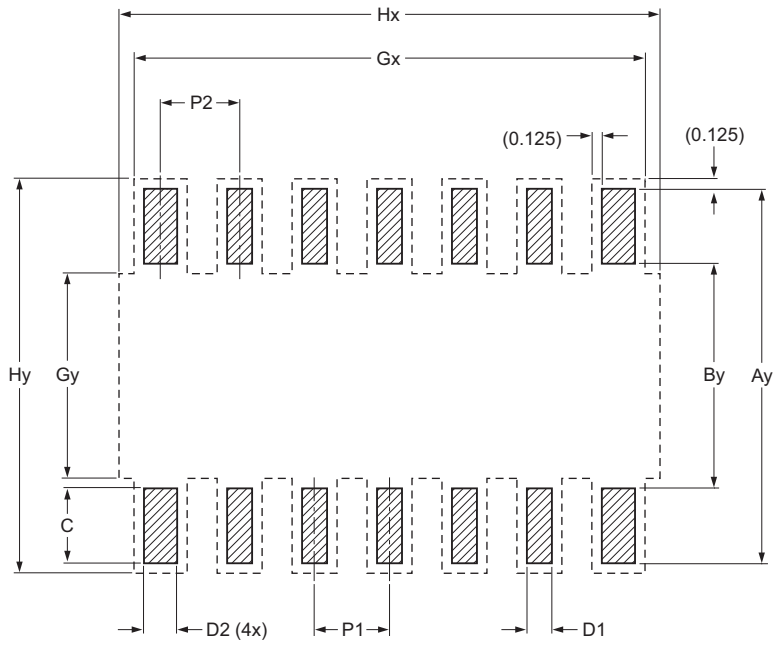


Fig 31. PCB footprint for SOT762-1 (DHVQFN14); reflow soldering

Footprint information for reflow soldering of TSSOP14 package **SOT402-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	4.950	5.300	5.800	7.450

sot402-1_fr

Fig 32. PCB footprint for SOT402-1 (TSSOP14); reflow soldering

19. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
FM	Frequency Modulation
GPIO	General Purpose Input/Output
GPS	Global Positioning Satellite
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
ID	Identification
LED	Light Emitting Diode
LSB	Least Significant Bit
MP3	MPEG audio layer 3
MSB	Most Significant Bit
SMBus	System Management Bus

20. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9571 v.1	20141222	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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