Document Number: MMRF1015N
Rev. 0, 7/2014

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for Class A or Class AB power amplifier applications with frequencies up to 2000 MHz. Suitable for analog and digital modulation and multicarrier amplifier applications.

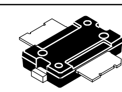
- Typical Two-Tone Performance at 960 MHz: V_{DD} = 28 Vdc, I_{DQ} = 125 mA, P_{out} = 10 W PEP
  - Power Gain — 18 dB
  - Drain Efficiency — 32%
  - IMD — -37 dBc
- Capable of Handling 10:1 VSWR @ 28 Vdc, 960 MHz, 10 W CW Output Power

Features

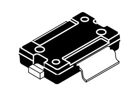
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip RF Feedback for Broadband Stability
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- 225°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units, 24 mm Tape Width, 13-inch Reel.

MMRF1015NR1
MMRF1015GNR1

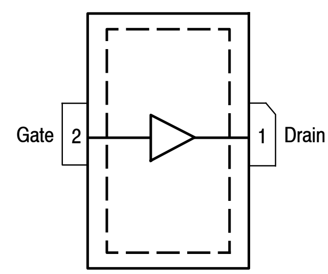
1-2000 MHz, 10 W, 28 V
CLASS A/AB
RF POWER MOSFETs



TO-270-2
PLASTIC
MMRF1015NR1



TO-270G-2
PLASTIC
MMRF1015GNR1



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 10 W PEP	$R_{\theta JC}$	2.85	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	1A
Machine Model (per EIA/JESD22–A115)	A
Charge Device Model (per JESD22–C101)	III

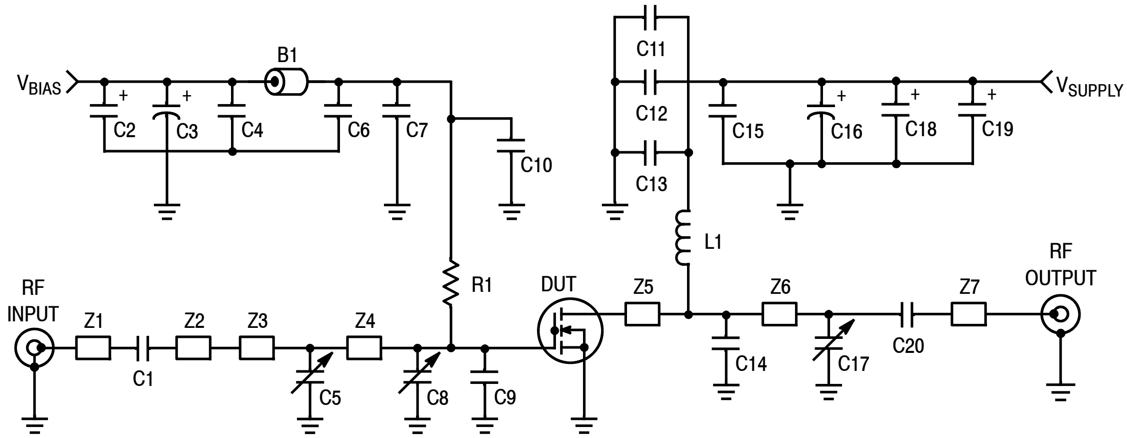
Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	1.5	2.3	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 125 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	3.1	4	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.3 Adc)	$V_{DS(on)}$	0.15	0.27	0.35	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.32	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	10	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	23	—	pF
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 125 mA, P_{out} = 10 W PEP, f = 960 MHz, Two–Tone Test, 100 kHz Tone Spacing					
Power Gain	G_{ps}	17.5	18	20.5	dB
Drain Efficiency	η_D	31	32	—	%
Intermodulation Distortion	IMD	—	–37	–33	dBc
Input Return Loss	IRL	—	–18	–10	dB
Typical Performance (In Freescale 450 MHz Demo Board, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 150 mA, P_{out} = 10 W PEP, 420–470 MHz, Two–Tone Test, 100 kHz Tone Spacing					
Power Gain	G_{ps}	—	20	—	dB
Drain Efficiency	η_D	—	33	—	%
Intermodulation Distortion	IMD	—	–40	—	dBc
Input Return Loss	IRL	—	–10	—	dB

1. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.



Z1	0.073″ x 0.223″ Microstrip	Z5	0.313″ x 0.902″ Microstrip
Z2	0.112″ x 0.070″ Microstrip	Z6	0.073″ x 1.080″ Microstrip
Z3	0.213″ x 0.500″ Microstrip	Z7	0.073″ x 0.314″ Microstrip
Z4	0.313″ x 1.503″ Microstrip	PCB	Rogers ULTRALAM 2000, 0.031″, ε_r = 2.55

Figure 2. MMRF1015NR1 Test Circuit Schematic — 900 MHz

Table 6. MMRF1015NR1 Test Circuit Component Designations and Values — 900 MHz

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead	2743019447	Fair-Rite
C1, C6, C11, C20	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C2, C18, C19	22 μF, 35 V Tantalum Capacitors	T491D226K035AT	Kemet
C3, C16	220 μF, 63 V Electrolytic Capacitors, Radial	2222-136-68221	Vishay
C4, C15	0.1 μF Chip Capacitors	CDR33BX104AKWS	Kemet
C5, C8, C17	0.8-8.0 pF Variable Capacitors, Gigatrim	272915L	Johanson
C7, C12	24 pF Chip Capacitors	ATC100B240JT500XT	ATC
C9, C10, C13	6.8 pF Chip Capacitors	ATC100B6R8JT500XT	ATC
C14	7.5 pF Chip Capacitor	ATC100B7R5JT500XT	ATC
L1	12.5 nH Inductor	A04T-5	Coilcraft
R1	1 kΩ, 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay

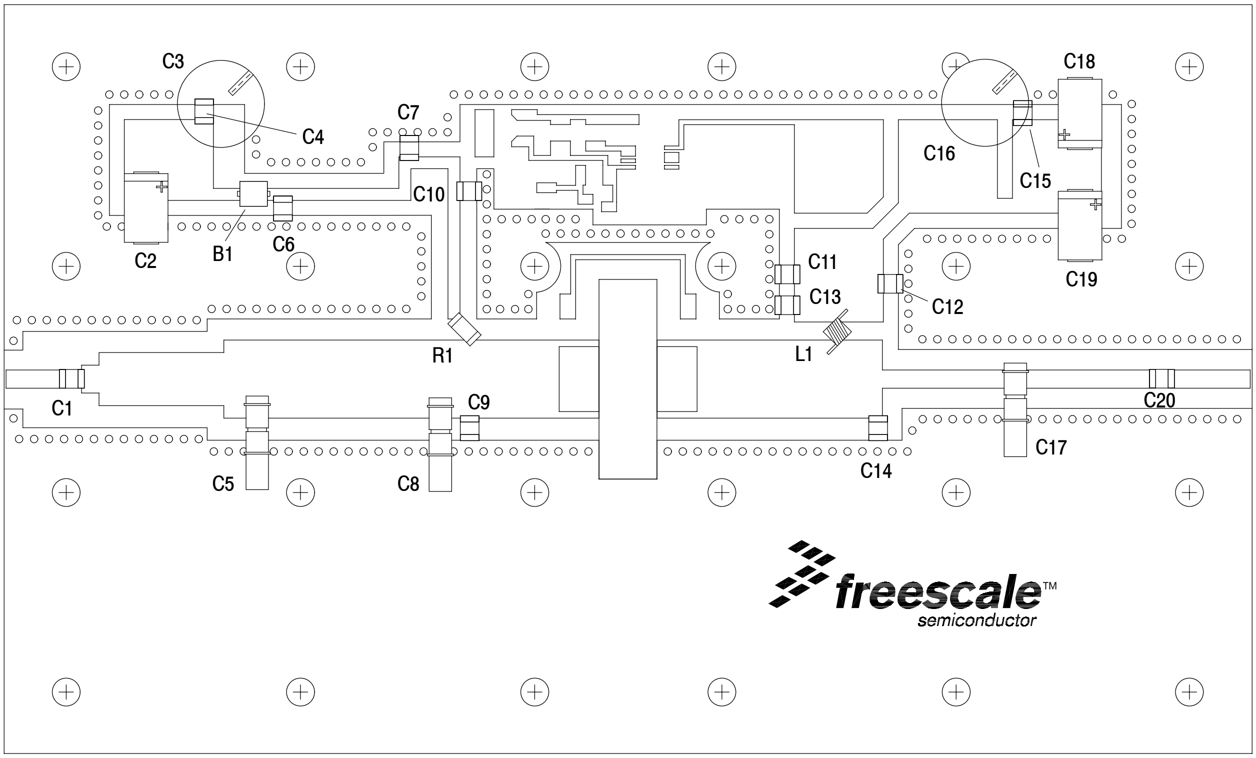


Figure 3. MMRF1015NR1 Test Circuit Component Layout — 900 MHz

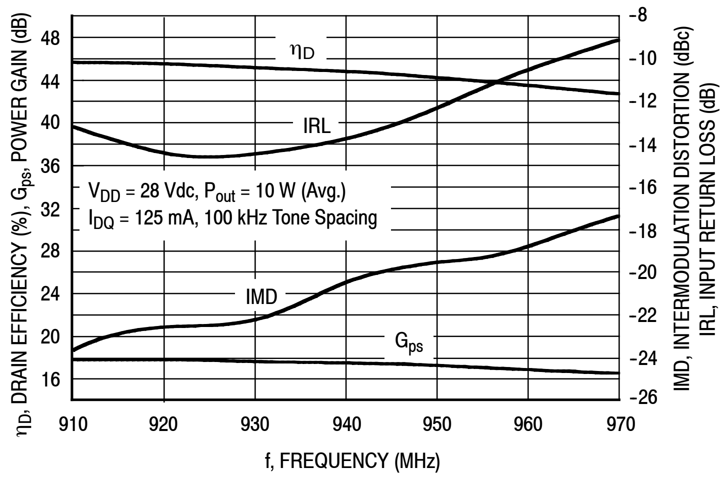


Figure 4. Two-Tone Wideband Performance @ P_{out} = 10 Watts

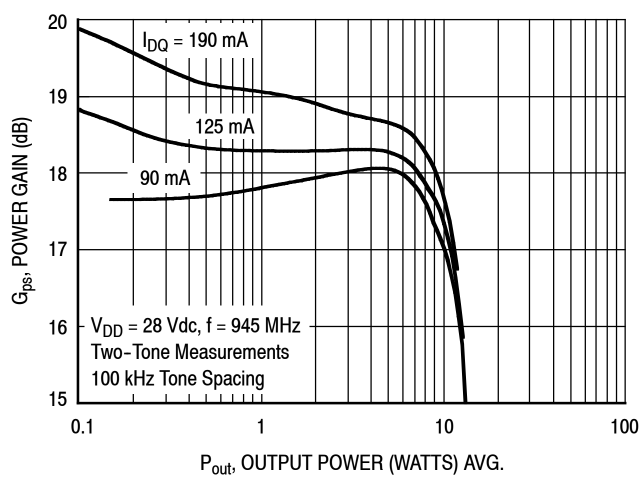


Figure 5. Two-Tone Power Gain versus Output Power

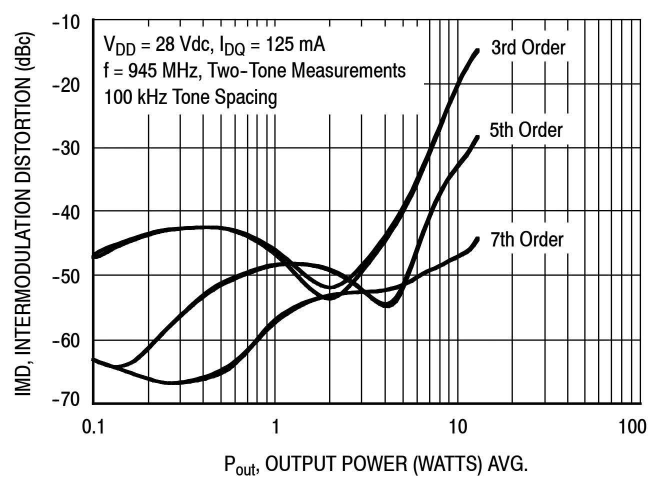


Figure 6. Intermodulation Distortion Products versus Output Power

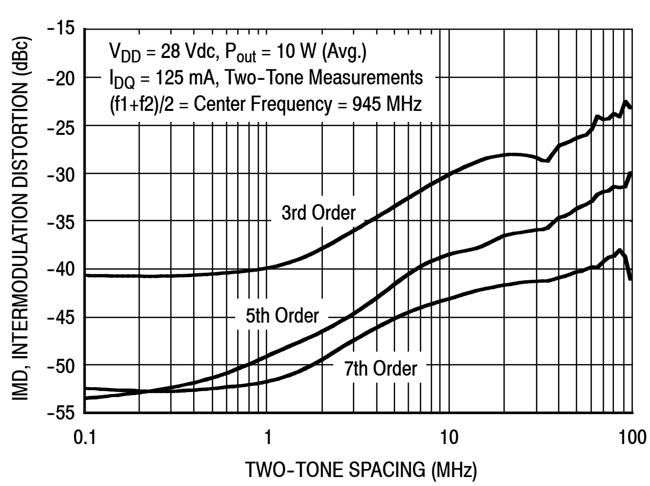


Figure 7. Intermodulation Distortion Products versus Tone Spacing

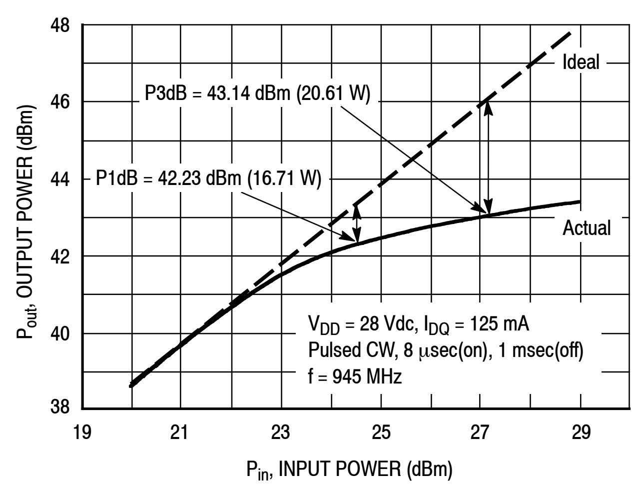


Figure 8. Pulse CW Output Power versus Input Power

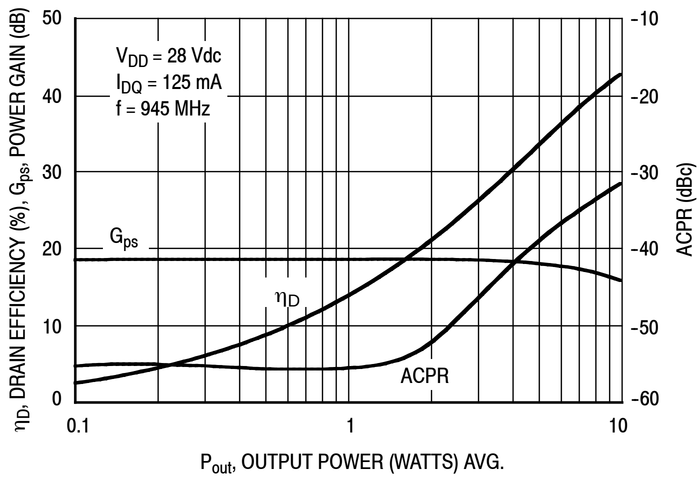


Figure 9. Single-Carrier CDMA ACPR, Power Gain and Power Added Efficiency versus Output Power

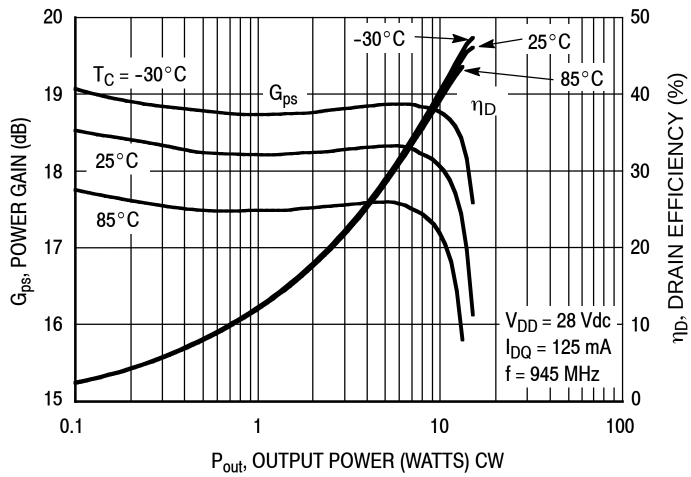


Figure 10. Power Gain and Power Added Efficiency versus Output Power

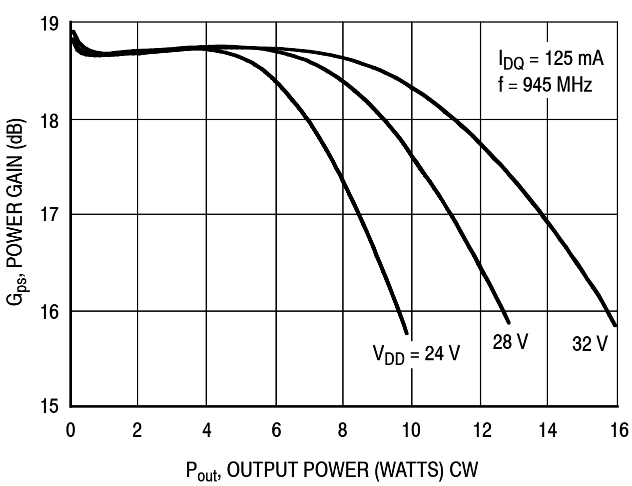


Figure 11. Power Gain versus Output Power

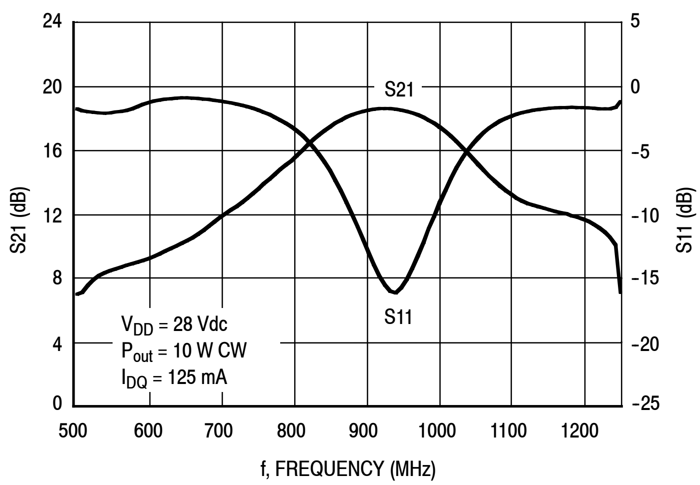
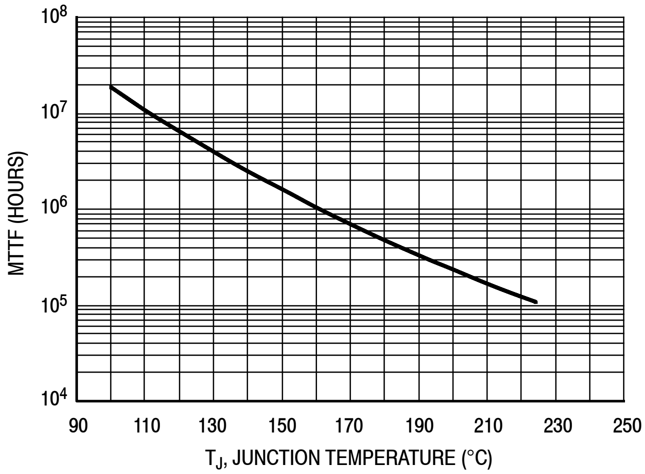


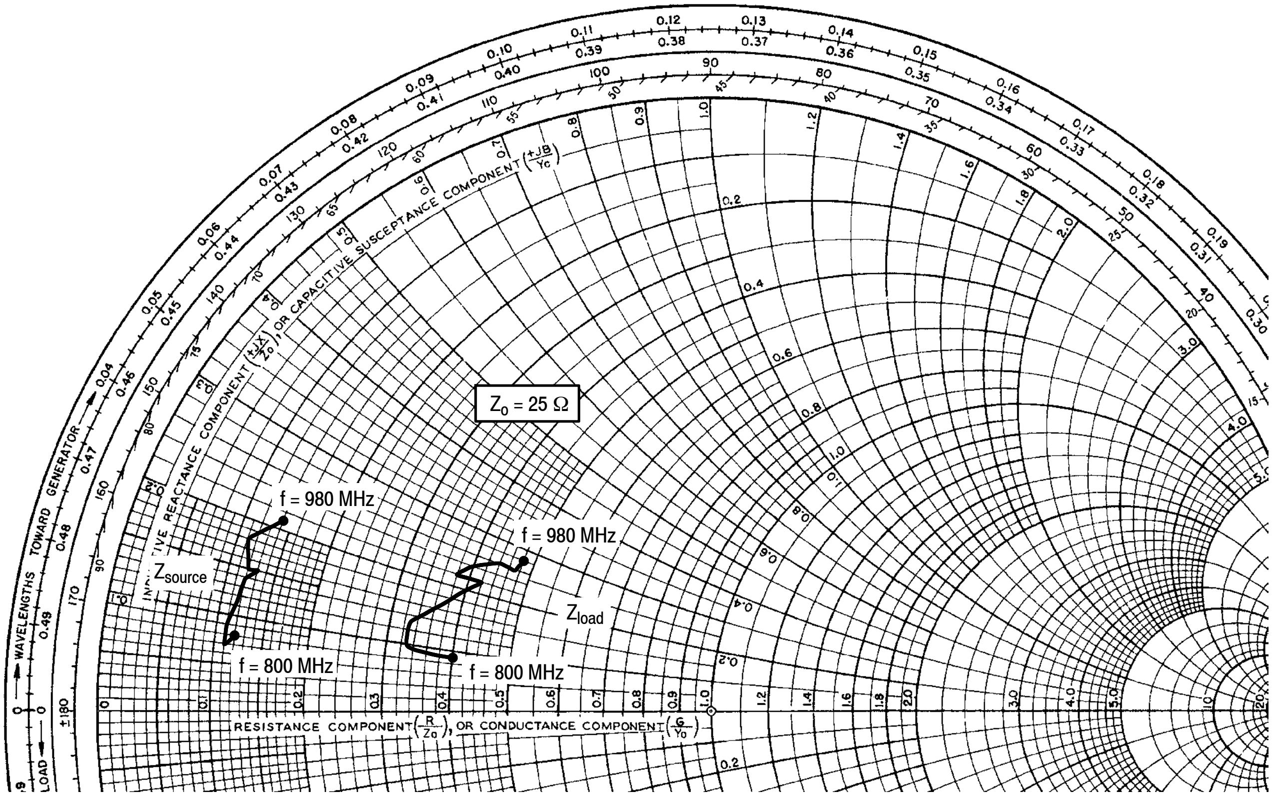
Figure 12. Broadband Frequency Response



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 10 W PEP, and η_D = 32%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF Factor versus Junction Temperature



V_{DD} = 28 Vdc, I_{DQ} = 125 mA, P_{out} = 10 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
800	3.1 + j1.9	10.1 + j2.3
820	2.8 + j1.7	8.3 + j2.5
840	2.7 + j2.2	8.2 + j3.3
860	3.1 + j3.4	9.8 + j4.8
880	3.3 + j3.8	10.6 + j5.6
900	2.9 + j3.7	9.5 + j5.5
920	2.8 + j4.4	10.1 + j5.9
940	3.0 + j4.7	11.0 + j6.4
960	3.2 + j4.9	11.8 + j6.6
980	3.6 + j5.2	12.1 + j7.1

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

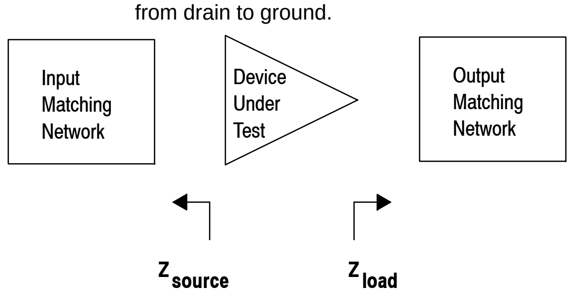
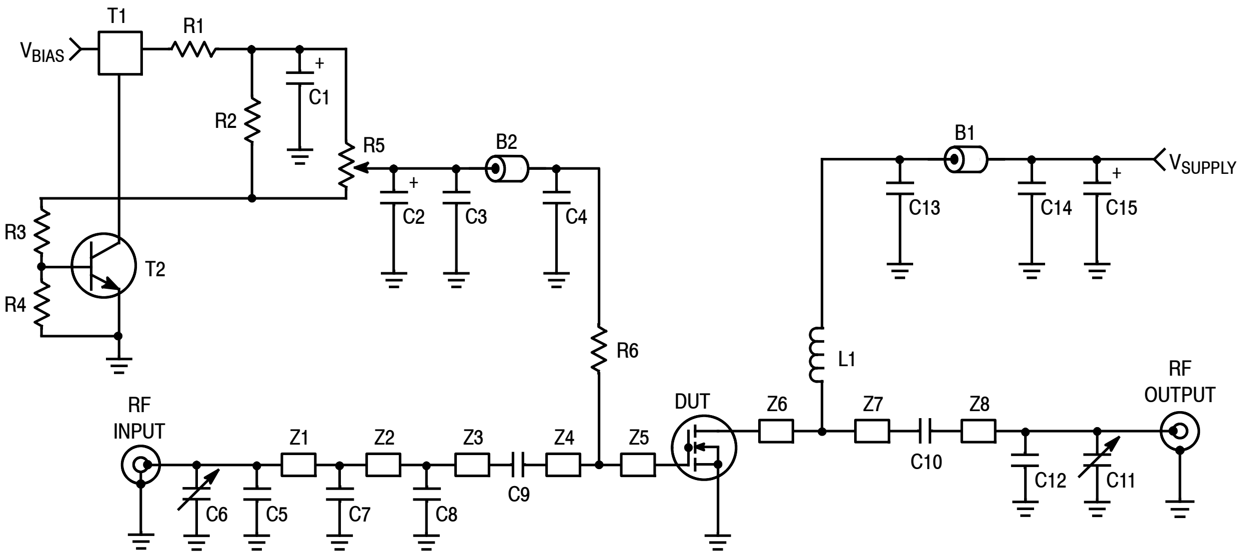


Figure 14. Series Equivalent Source and Load Impedance — 900 MHz



Z1	0.540″ x 0.080″ Microstrip	Z5	0.475″ x 0.330″ Microstrip
Z2	0.365″ x 0.080″ Microstrip	Z6	0.475″ x 0.325″ Microstrip
Z3	0.225″ x 0.080″ Microstrip	Z8	1.250″ x 0.080″ Microstrip
Z4, Z7	0.440″ x 0.080″ Microstrip	PCB	Rogers ULTRALAM 2000, 0.030″, ε_r = 2.55

Figure 15. MMRF1015NR1 Test Circuit Schematic — 450 MHz

Table 7. MMRF1015NR1 Test Circuit Component Designations and Values — 450 MHz

Part	Description	Part Number	Manufacturer
B1, B2	Ferrite Bead	2743019447	Fair–Rite
C1	1 μF, 35 V Tantalum Capacitor	T491C105K050AT	Kemet
C2, C15	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C3, C14	0.1 μF Chip Capacitors	C1210C104K5RAC	Kemet
C4, C9, C10, C13	330 pF Chip Capacitors	ATC700A331JT150XT	ATC
C5	4.3 pF Chip Capacitor	ATC100B4R3JT500XT	ATC
C6, C11	0.6–8.0 pF Variable Capacitors	27291SL	Johanson
C7, C8, C12	4.7 pF Chip Capacitors	ATC100B4R7JT500XT	ATC
L1	39 μH Chip Inductor	ISC–1210	Vishay
R1	10 Ω Chip Resistor	CRCW080510R0FKEA	Vishay
R2	1 kΩ Chip Resistor	CRCW08051001FKEA	Vishay
R3	1.2 kΩ Chip Resistor	CRCW08051201FKEA	Vishay
R4	2.2 kΩ Chip Resistor	CRCW08052201FKEA	Vishay
R5	5 kΩ Potentiometer	1224W	Bourns
R6	1 kΩ Chip Resistor	CRCW12061001FKEA	Vishay
T1	5 Volt Regulator, Micro 8	LP2951CDMR2G	On Semiconductor
T2	NPN Transistor, SOT–23	BC847ALT1G	On Semiconductor

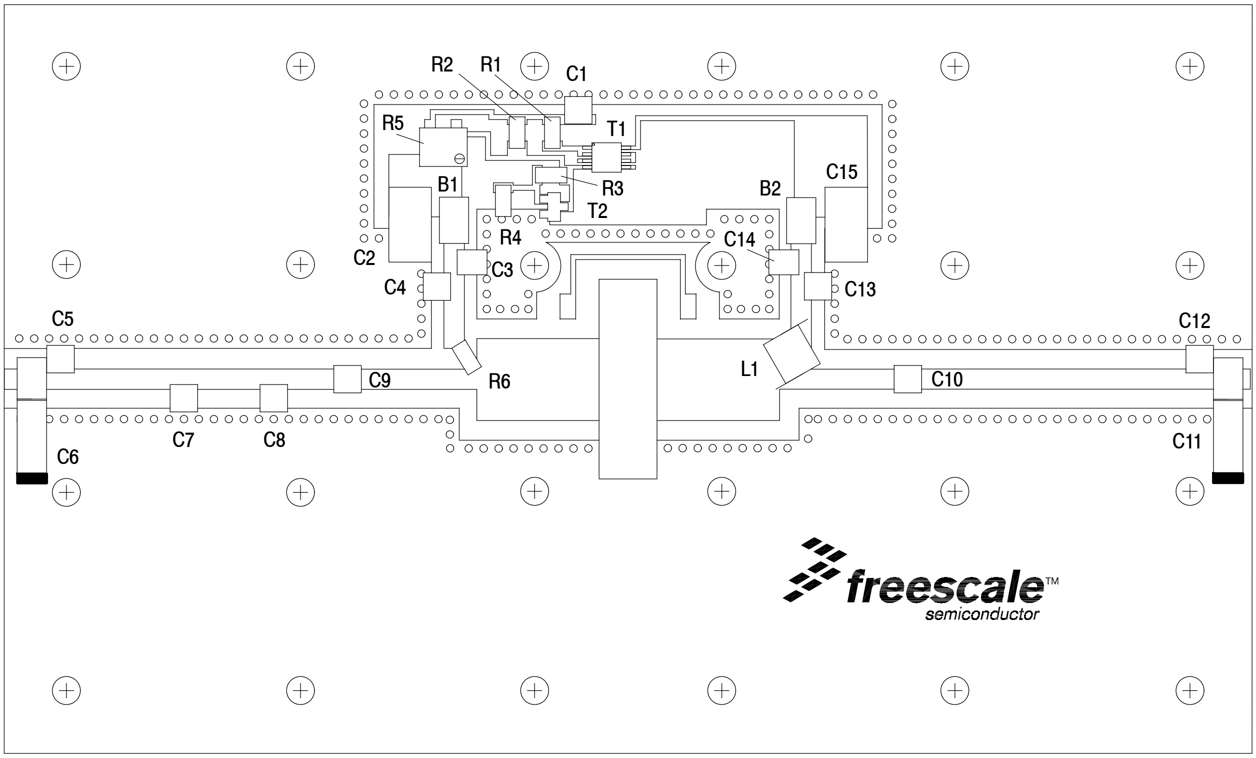


Figure 16. MMRF1015NR1 Test Circuit Component Layout — 450 MHz

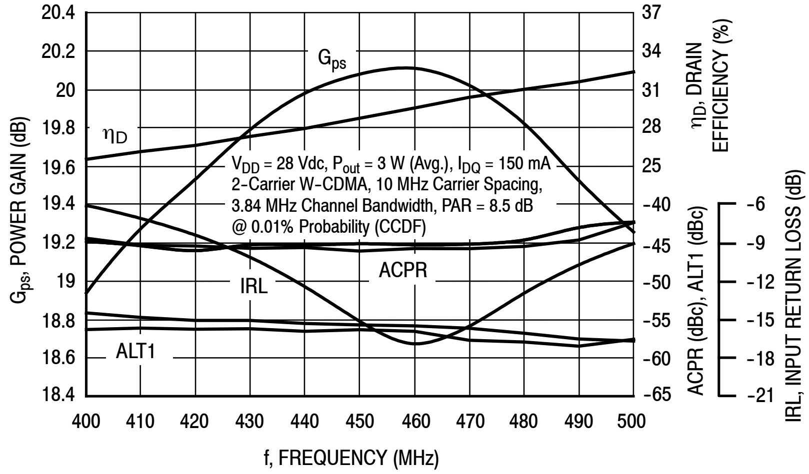


Figure 17. 2-Carrier W-CDMA Broadband Performance @ P_{out} = 3 Watts Avg.

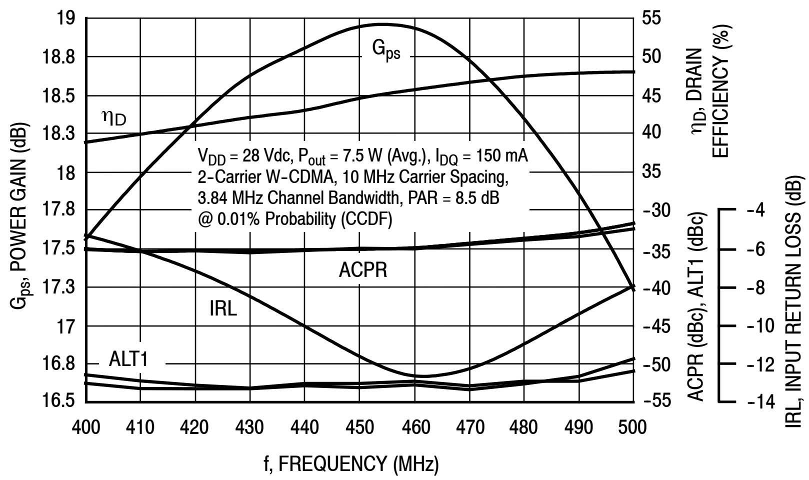


Figure 18. 2-Carrier W-CDMA Broadband Performance @ P_{out} = 7.5 Watts Avg.

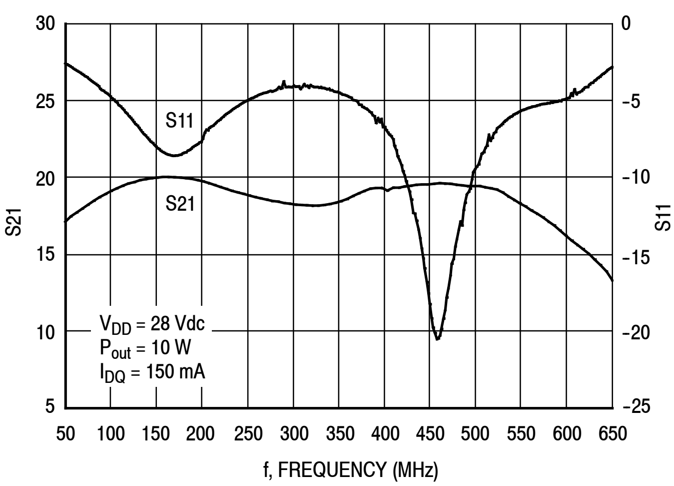


Figure 19. Broadband Frequency Response

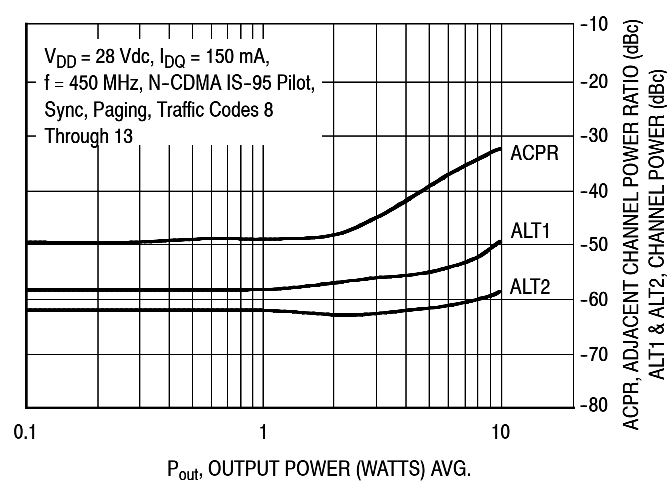
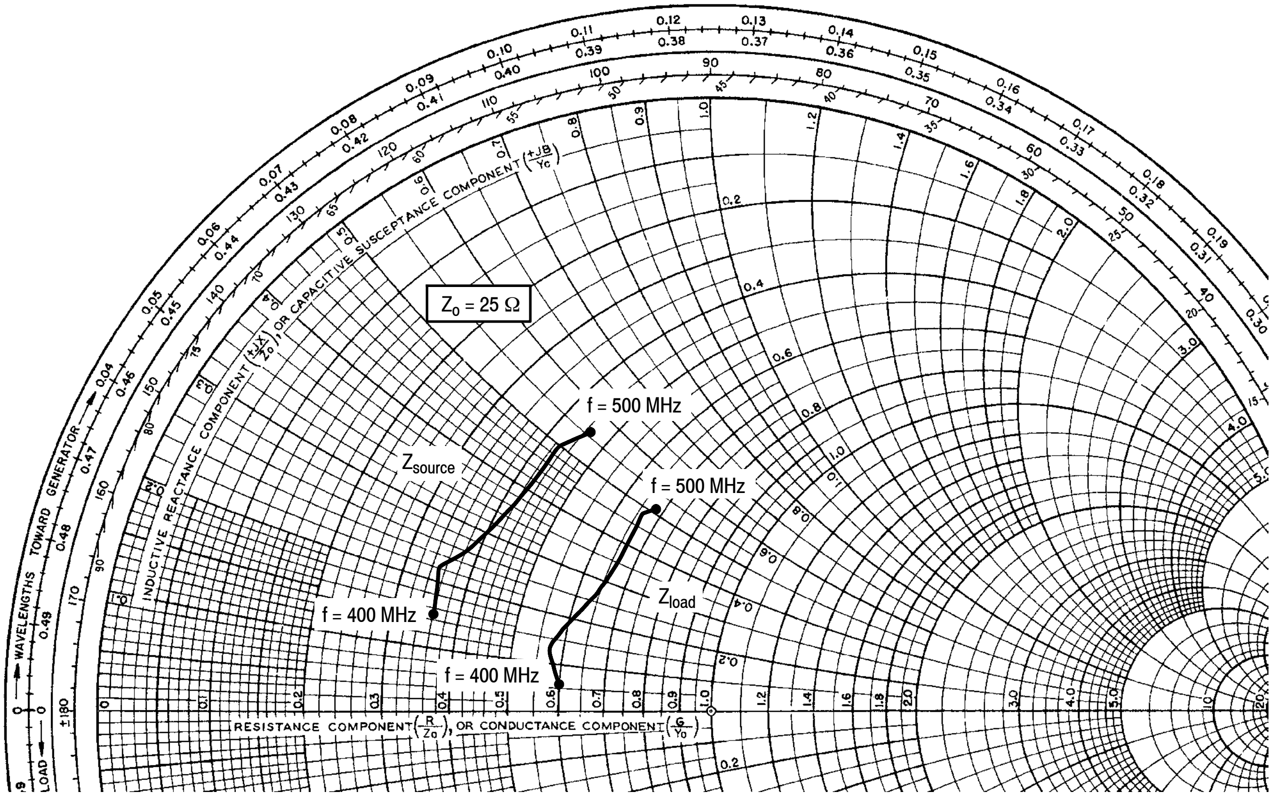


Figure 20. Single-Carrier N-CDMA ACPR, ALT1 and ALT2 versus Output Power



V_{DD} = 28 Vdc, I_{DQ} = 150 mA, P_{out} = 10 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
400	9.0 + j3.8	15.0 + j1.4
420	8.8 + j5.4	14.3 + j3.3
440	9.6 + j6.6	15.0 + j4.7
460	10.6 + j9.5	16.3 + j7.3
480	10.7 + j12.6	16.4 + j11.1
500	11.5 + j13.9	16.9 + j12.7

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

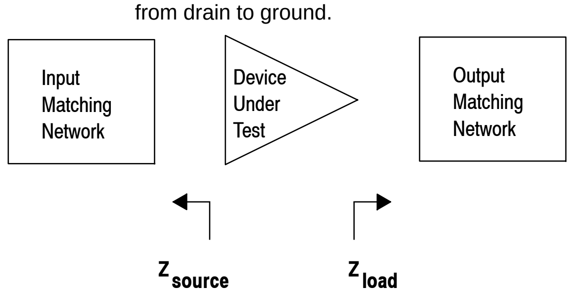
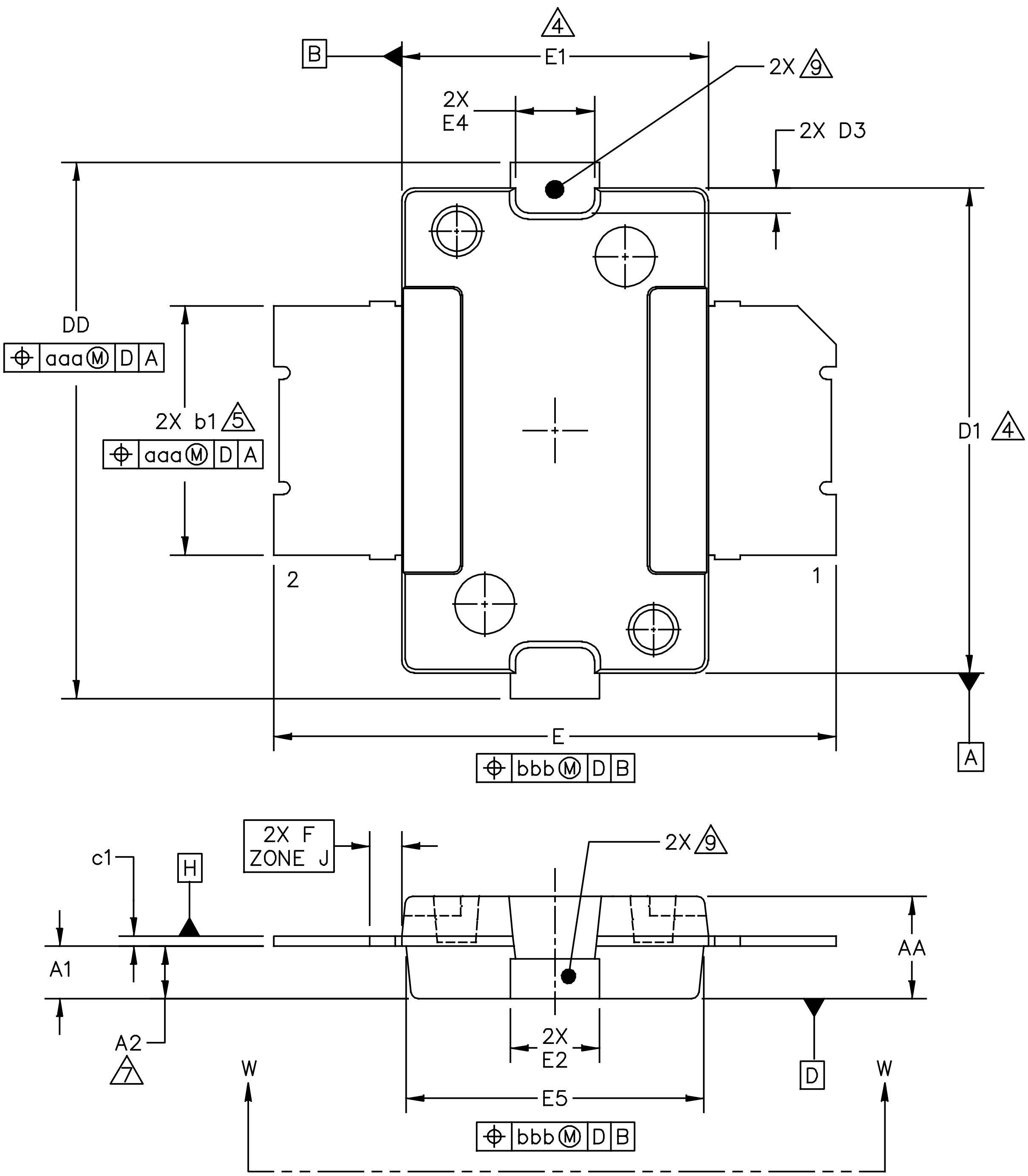


Figure 21. Series Equivalent Source and Load Impedance — 450 MHz

PACKAGE DIMENSIONS



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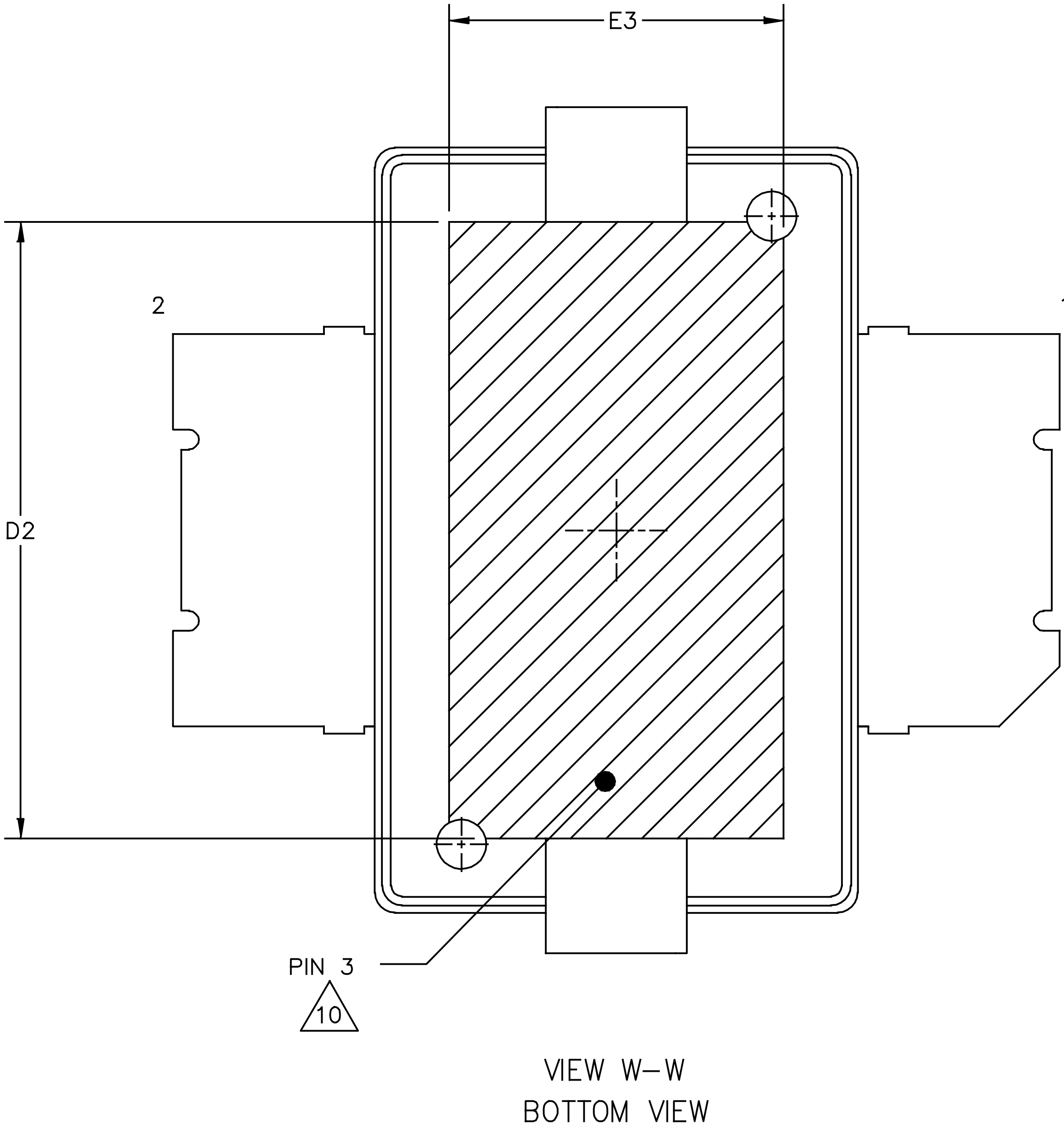

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	STANDARD: NON–JEDEC	
	02 JUN 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. DIMENSIONS DD AND E2 DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH (10.92 MM) FOR DIMENSION DD AND 0.080 INCH (2.03 MM) FOR DIMENSION E2. DIMENSIONS DD AND E2 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE D.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

10. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. DIMENSIONS D2 AND E3 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.078	.082	1.98	2.08	E4	.058	.066	1.47	1.68
A1	.039	.043	0.99	1.09	E5	.231	.235	5.87	5.97
A2	.040	.042	1.02	1.07	F	.025 BSC		0.64 BSC	
DD	.416	.424	10.57	10.77	b1	.193	.199	4.90	5.06
D1	.378	.382	9.60	9.70	c1	.007	.011	0.18	0.28
D2	.290	----	7.37	----	aaa	.004		0.10	
D3	.016	.024	0.41	0.61	bbb	.008		0.20	
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					

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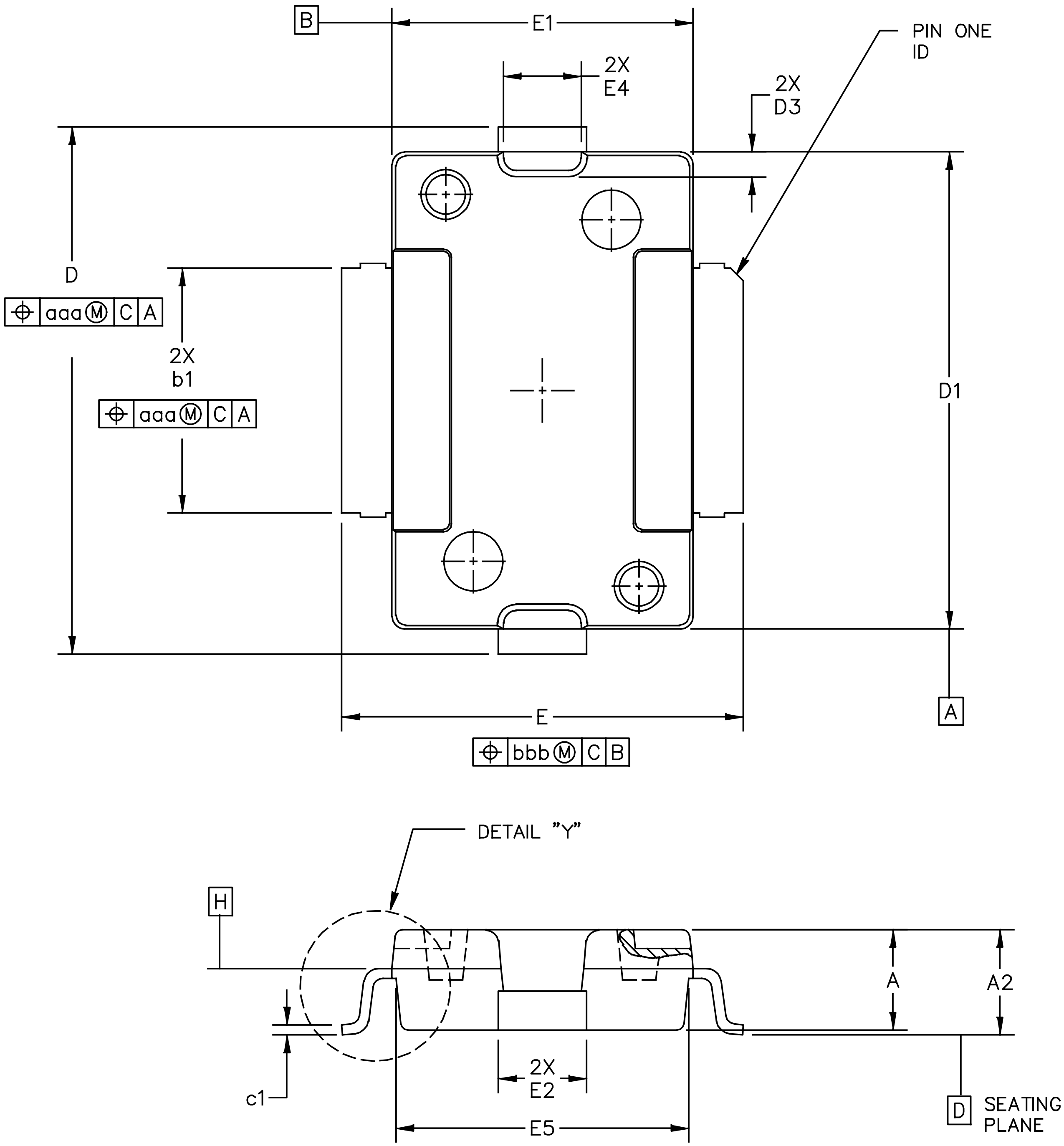

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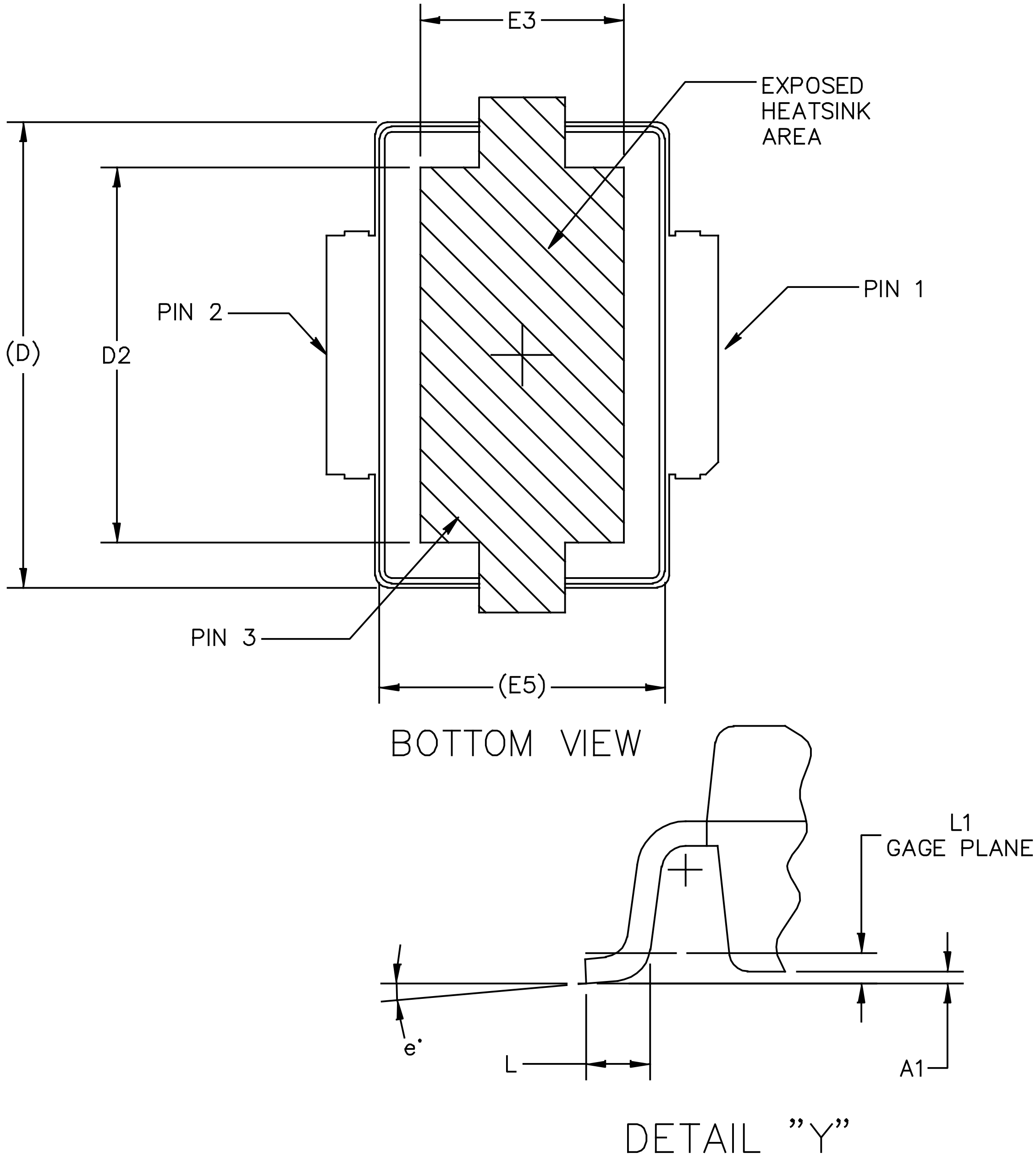

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	STANDARD: JEDEC TO–270 BA	

NOTES:

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3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –D–.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.01 BSC		0.25 BSC	
A2	.077	.088	1.96	2.24	b1	.193	.199	4.90	5.06
D	.416	.424	10.57	10.77	c1	.007	.011	0.18	0.28
D1	.378	.382	9.60	9.70	e	2°	8°	2°	8°
D2	.290	–	7.37	–	aaa	.004		0.10	
D3	.016	.024	0.41	0.61					
E	.316	.324	8.03	8.23					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	–	3.81	–					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: TO–270 GULL WING	DOCUMENT NO: 98ASA99301D	REV: C
	CASE NUMBER: 1265A–03	02 JUL 2007
	STANDARD: JEDEC TO–270 BA	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2014	• Initial Release of Data Sheet

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